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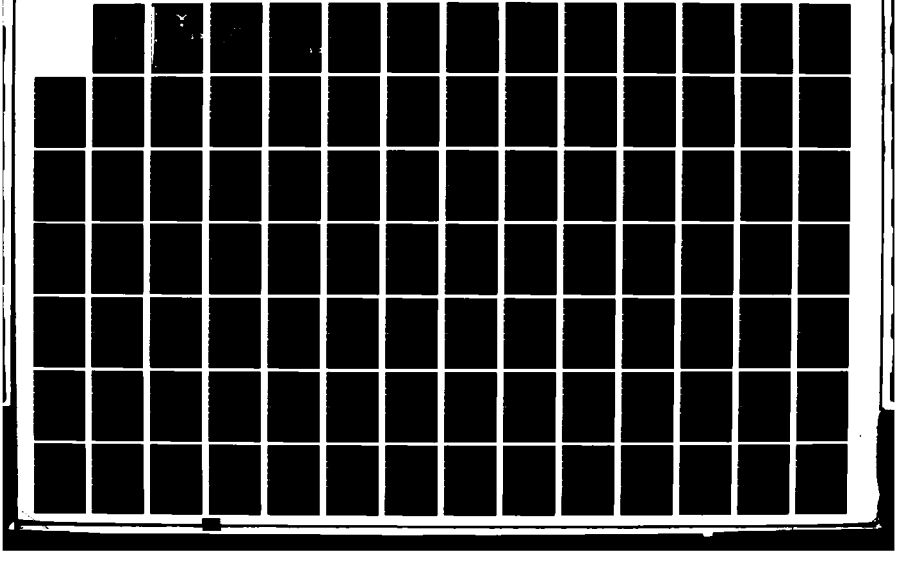

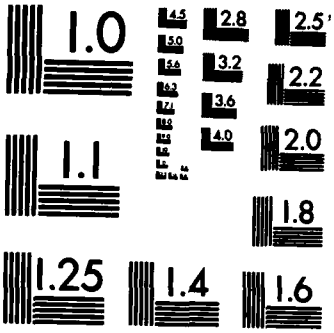

CONTINUED DEVELOPMENT
OF THE
UNIVERSAL NETWORK INTERFACE DEVICE

THESIS

AFIT/GE/EE/82D-28

Gennaro [illegible]
Capt. USAF

DEPARTMENT OF THE AIR FORCE
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CONTINUED DEVELOPMENT

OF THE

UNIVERSAL NETWORK INTERFACE DEVICE

THESIS

Presented to the Faculty of the School of Engineering

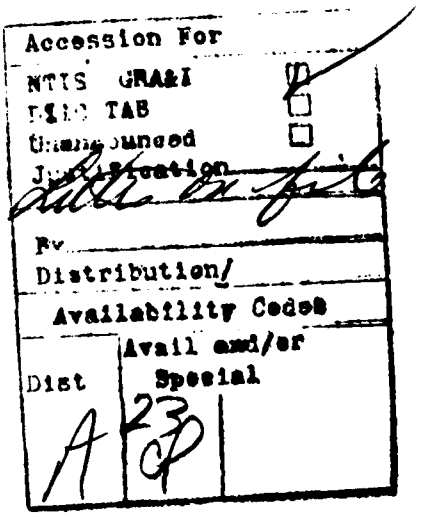
of the Air Force Institute of Technology

Air University

in Partial Fulfillment of the

Requirements for the Degree of

Master of Science



by

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Graduate Electrical Engineering

December 1982

Preface

The purpose of this investigation was to continue the development of the Universal Network Interface Device (UNID). This involved the design and construction of a new memory board which incorporated two previously constructed memory boards. This investigation was limited to the development and testing of that new board and the UNID itself.

I would like to thank my thesis advisor, Dr. Gary Lamont, for his assistance and encouragement during the course of this investigation. I would also like to thank my readers for their valuable comments and aid in this study. The high quality support of the lab engineers and technicians saved me much valuable time and I would like to thank in particular, Capt. Lee Baker, Dan Zambon, and Orville Wright for their excellent support during the construction and testing phases of this study. Finally, I wish to acknowledge my gratitude to my wife, Linda, for her encouragement and understanding during this effort.

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Abstract

The objective of this investigation was to design and construct two memory boards for the Digital Engineering Laboratory Network's (DELNET's) Universal Network Interface Devices (UNIDs). The UNID is a flexible message processor designed for computer communications network applications. The new memory boards incorporated the prototype microcomputer based message processor memory boards of the previous theses. Using the existing memory boards, new memory boards were designed, constructed, tested, and documented. The results of this effort were the elimination of unreliable RAM, the reduction in the number of circuit boards used in the UNID, and two operational UNIDs.

CONTINUED DEVELOPMENT OF THE UNIVERSAL NETWORK INTERFACE DEVICE

I. Introduction

The purpose of this investigation was to continue the development of an operational microcomputer based message processor with the inherent flexibility to permit its utilization in different types of data communications network applications. The need for a universal network device was first proposed by the Air Force Communication Service (AFSC) (28). There have been four previous investigations (22,5,1,17) into the development of a universal network interface device, and this investigation represents the fifth phase of the study effort towards an operating device.

The remaining sections of this chapter will address background information, followed by the scope, approach, and overview of the work covered in this thesis.

Background

Computer network theory and application, as developed over the past decade, enjoys widespread attention today. Computer networks have become an attractive alternative for increasing computational power and sharing computer resources. Undoubtedly the most successful example of computer networks is the current Defense Advanced Research Project Agencies Network (ARPANET). This packet switched network not only represents the future of computer

but also establishes network theory for later applications (14:5-23). One application of that theory is the CSNET (Computer Science Network). While the ARPANET is, or at least tries to be, a closed society limited to people who are working on Department of Defense contracts, CSNET to provide network services to the entire U.S. computer . ence community (2).

Unfortunately, an international network of thi .ize cannot be tailored to the needs of all potential network users. Using the ARPANET as a simple computer network interconnecting various minicomputers and microcomputers is impractical. These machines may not need the resources available through the ARPANET. A cost-effective and efficient computer network, dedicated to these smaller machines, would be more desirable. Such a computer network is commonly known as a local network (23:286-323).

Local networks tailored to a particular organization and interconnecting minicomputers became practical with the advent of the microprocessor. The microprocessor was the first development in support of local networks because it allowed economic network nodes to be developed. These nodes were cost-effective and yet offloaded much of the network protocol processing overhead from the computer hosts on the network. This made it practical for organizations to use a local network of microcomputers in lieu of time-sharing mainframe computer.

A second fortunate development in support of

networks was research into the design of routing algorithms and the techniques of flow control. Obviously, routing algorithms and flow control have direct impact on local network applications. An efficient routing algorithm insures that messages reach their destinations with a minimum delay (20:213-241). Likewise, sound flow control techniques will limit congestion on the network (20:242-258). Currently, these research efforts are yielding positive results for network applications.

A third important development for local networks came with an understanding of the need for network protocols. Protocols permit one machine to communicate with another machine through rules governing the timing and formatting of the data to be exchanged (13:35). Many different protocols and associated levels are now available with some movement toward standardization. The first protocols were developed as part of scientific research projects under ARPANET and the French Cyclades network (13:67-69). Commercial manufacturers have also developed various protocols. IBM developed the binary synchronous communication (BISYNC) protocol (23:190) and the System Network Architecture (SNA) (13:70), and DEC introduced DECnet (Digital Equipment Corporation network) (13:69-70). These are examples of machine dependent local networks.

However, within the last four years, more flexible local networks have become available. These networks are designed to interface many different types of machines. Typical

examples are Ungermann-Bass's NET/ONE and Xerox's ETHERNET (15,3). NET/ONE uses a network interface unit (NIU) built around the Z80A microprocessor. The transmission medium is a baseband coaxial cable capable of transmission speeds up to 4 Mbps. The NIU is a significant feature of this network. A single NIU can connect to the network any one of a large number of dissimilar machines. Reconfiguration of the NIU for different machines is accomplished easily by loading different software. Additionally, each NIU is isolated from the network. Should one NIU fail, the rest of the network will not be affected. Further, NET/ONE NIUs contain most of the network protocols, making the network operation essentially transparent to both the user and the host (3).

The ETHERNET is similar to NET/ONE, but not as resourceful (15). ETHERNET does not use network interface units. This requires the subscriber to house the network overhead in his machine. Instead, a transceiver interfaces each user to the network. This transceiver isolates the network from user faults as well as connecting the user to the baseband cable.

A baseband cable uses a bidirectional signal path on which signals are encoded onto the cable. It only has one single data channel and must be supplemented with other [illegible] of wiring to provide non-data-communications need[illegible]. [illegible] the single data channel, baseband networks are [illegible] having data rates up to 10 Mbps over short distances [illegible] than 100 feet. Those distances can be extended to [illegible] Km,

but reduced data rates from the effects of dispersion results. This is in contrast to a broadband cable which is a unidirectional signal path. Both a transmit path and a receive path must exist. This is accomplished either by splitting the available bandwidth into transmit and receive channels on the same cable or by providing separate cables for signal transmission and reception. Broadband supports multi-mode communications, including audio, video, and data on one cable pathway. Broadband networks have greater distance capability (from over 1000 feet up to several miles) while retaining full bandwidth because they use active amplifiers to distribute and extend the signal range. Broadband allows for greater distances than baseband but the data-rate decreases below 10 Mbps after several miles (12).

In many countries, the government or private industry began offering network services to any organization that wished to subscribe (23:28). These networks are called public networks similar to, and often part of, the public telephone and utilities systems. Such widely available networks needed common agreement on some form of protocol. With this approach many users operating dissimilar hardware could subscribe to this service. In an effort to provide standardized and compatible services throughout the world, these countries cooperate through the International Telephone and Telegraph Consultative Committee (CCITT) to issue "recommendations" for providing various types and levels of service (23:97). Several recommendations for

switching network operations have been adopted in recent years, such as IBM's SNA, DEC's DECnet, Honeywell's Distributed Systems Environment (DSE), the United Kingdom's National Physics Laboratory (NPL) net and France's Cyclades net (4). Most notably is the X.25 recommendation specifying the interface or protocol to be voluntarily adopted by all manufacturers and users (13:71-73).

As local networks became more efficient and better understood, the U. S. Air Force began evaluating their potential usefulness. In the past, telecommunications requirements on an Air Force base were met in a single and straight forward manner by providing voice communications via telephone facilities, plus a few low-speed teletypewriter and data circuits over base cable systems (28:2). However, with the tendency toward use of digital processors to accomplish base-level functions, the base-level telecommunication facilities needed to be reevaluated to insure they could support the increased data communications needs (28:2). This reevaluation was accomplished in the 1842 EEG/EEIC technical report TR 78-5 (28).

One facet of the TR 78-5 technical report involved the method of accomplishing the base-level message and its switching and distribution functions. At the base level, distribution of data and of other traffic is an important consideration since it encompasses user terminals and the communication paths connecting them into the base level network. There are, in general, more user terminals

anything else in the network and thus costs associated with them are multiplied by a large factor.

To satisfy the base-level message and data switching, and distribution functions, the report postulated the need to connect any of the base digital processing devices to any terminal on the base and also the need to connect any base terminal to any other base terminal. To accomplish this interconnection, the "1842" report suggested three different types of network interconnections; the first was a star communication network with a centralized digital switch (28:162-163); the second was based upon the concepts used in the Advanced Research Project Agency (ARPA) network (28:164), and the last was the loop or ring network (28:164). The configuration the report finally recommended for the base-level data distribution network was a modification to the ring concept called a multi-ring network. This network consisted of a number of ring networks with a node providing interconnectivity between the rings. This multi-ring network concept offered particular advantages in terms of cost, development, application, and flexibility. A key to the multi-ring concept was the development of five types of devices which could interface the multiple rings together.

Rome Air Development Center was tasked with addressing the problem of the interface devices. It was recognized that the various interface devices proposed had similar features and were required to perform similar functions. Thus, it appeared reasonable that one universal network

device (UNID) could be developed which could meet the separate requirements of each of the five proposed interface devices of the multi-ring concept. The subsequent development of the UNID and a local network application became the basis for numerous investigations. A preliminary design for the UNID was written in 1978 (22). The building of a prototype UNID based on this design was begun in 1979 (5). In 1980, the building of the prototype continued, modifications added, and the design refined (1). Also in 1980, the development and design of a local computer network for AFIT's Digital Engineering Laboratory Network (DELNET) was begun using the UNID and the loop network concepts (11). In 1981, concurrent investigations (9,17) continued development of the software for the DELNET, finished constructing the prototype UNID, built a second UNID, and implemented a prototype DELNET.

The two UNIDs were used as nodes, forming a simple local network following a previous design (11). The prototype network included two computers and several terminals using a fiberoptic communications link. The major components of each UNID were a card cage, motherboard, local processor card, network processor card, shared memory card, system memory card, local card, and network card (17:23).

At present, a concurrent investigation continues development of software for DELNET (10). Finally, an investigation, completed in 1982, alleviates the problem which the previous thesis had with random access memory.

numerous quantity of dynamic RAM chips used in the system memory produced transient signals caused by the continual refresh. Circuit coupling and switching noise due to the wire wraps also created problems.

Scope

The basic hardware for the UNID is constrained by the design and implementation of previous investigators. This investigation remained within these constraints and continued the development of the UNID. The recommendations in previous theses were identified and implemented. These resulted in the design and implementation of a new memory board which combines the shared memory board with the system memory board.

This investigation elected to concentrate on hardware implementation and to write software only as necessary to test that implementation. A co-investigator (10) supplied most of the software support. Previously developed software was also used.

The development of the UNID suffered from the lack of current documentation. This investigation updated all cable connections, schematics, lists, etc., necessary for further development. This information is contained in the appendicies.

Approach

First, an operable UNID was needed. At the beginning of this investigation no such UNID was available due to [illegible] failures. Next, the memory boards were reconfigured [illegible]

static RAM chips, reducing the number of ICs and eliminating the circuit coupling and switching noise associated with the wire wraps. The reduction in ICs also eliminated the transient signals, caused by the continual refresh, which were seriously affecting the reliability of memory contents. Finally, both the system memory and shared memory boards were combined onto one memory board reducing 112 memory chips used to only 10 memory chips. Simple tests proved that the UNIDs memory was now reliable.

Overview

This report covers hardware aspects of the UNID. Chapter II presents a summary of established requirements and design followed by a discussion of modifications implemented during this investigation. Chapter III details all construction modifications made to the UNID. Hardware testing of components is documented in Chapter IV. Chapter V summarizes the results of this investigation and recommends areas for further study. Finally, the Appendicies contain all hardware documentation.

II. Requirements and Design

This chapter summarizes the requirements and design decisions established by previous theses (22,11,17). These requirements come from the initial design as discussed in Chapter I. These decisions formed the guidelines for this investigation. This chapter is divided into six sections: UNID requirements summary, DELNET requirements summary, DELNET design summary, UNID design summary, UNID implementation, and Documentation.

UNID Requirements Summary

In 1978, the 1842 EMG report was used to motivate the design of the UNID (22). The UNID, being universal, was based on the following general concepts (22:11-13):

-The UNID functions as a store-and-forward concentrator with message routing capability.

-The UNID includes specialized I/O ports to handle unique communication requirements.

-The UNID easily handles various network operating systems and communication protocols.

Using these concepts and structured analysis techniques (SAT), UNID functional requirements were developed (29,22:11-13). This approach developed an activity model consisting of a series of SAT diagrams showing the UNID functions and their interrelations. Below is an excerpt summarizing these functional requirements:

I. Communication Interface.

A. Flexibility.
B. Signal Characteristics.
C. Port Configuration.
D. Protocol Software.

II. Local Information Processing.

A. Receive local information.
B. Store information.
C. Process local information.
D. Transmit information to network.

III. Network Information Processing.

A. Receive information from network.
B. Process information from network.
C. Retransmit network information on network.
D. Transmit information to local receiver.

1. Process control information.
2. Transmit information to subscriber.

Once these general functional requirements were stated, broad UNID bounds necessary for subsequent function allocation and design phases were established. Below is a list of these initial system bounds. Justification is presented in (22:34-46).

-Unid modularity based on circuit cards.
-Software implementation of different protocols.
-Synchronous, serial data rates up to 1.5 Mbps.
-Minimum of one full complex network I/O port.
-RS-232C interfaces for local I/O ports.
-One local I/O port for 20 mA current loop.
-Interrupt controlled I/O ports.

The functional requirements allocation to UNID hardware and software was completed after establishing system bounds. At this point, three major components of the UNID were identified: local I/O, network I/O, and processor. The following lists summarize the allocation to these components (22:48-49).

Local I/O Component (Hardware)

Recognize start of local information.
Recognize end of local information.
Recognize end of local message.
Transmit local information.

Network I/O Component (Hardware)

Recognize start of network information.
Recognize end of network information.
Change serial information to parallel.
Transmit network information.

Processor Component (Software)

Information to be transmitted.

Store outgoing local information.
Convert to network character set.
Identify ready to be processed information.
Process information to be transmitted.
Determine routing.
Initialize transmitter.
Identify information as sent.
Deallocate storage space.

Information received.

Store incoming network information.
Determine if error free.
Process information from network.
Identify as ready to be transmitted.
Identify type of message.
Remove protocol information.
Process control information.
Transmit information to local subscriber.

Each entry corresponds to a particular diagram in the activity model (22:48-49).

DELNET Requirements Summary.

With the requirements of the UNTD complete, the [illegible] a UNTD based local network for AFIT's Digital [illegible] Laboratory was designed [illegible] then constructed [illegible]

(5,1,17). Two aspects of local networks motivated the investigation. First, local networks can increase processing power without adding more computers through resource sharing. Secondly, researchers and designers need a flexible local network testbed capable of supporting network theory development.

The DELNET design was a top down development using SAT. Design began by establishing user requirements for the development network in the Digital Engineering Laboratory. A three-part user survey established these requirements. The following is a summary of the most important requirements for the DELNET (11:19-23):

-Ability to transfer files across the network.
-Ability to share peripherals attached to other hosts on the network.
-Flexibility in network configuration and operation.
-High percentage of availability.
-Performance monitoring capability.

These functional requirements were then used to establish DELNET system requirements, including both hardware and software. The system hardware requirements were essentially common sense approaches to network topology, hosts, nodes, and transmission mediums (11:27-29). Topology must be flexible and easily expandable, [illegible] bottlenecks that limit throughput and response time. All computers, regardless of their sophistication, should be easily added to the network. Computers with [illegible] powerful and/or dedicated [illegible] should be [illegible].

nodes should not degrade host performance, keeping the DELNET nearly transparent to the user. Nodes must reconfigure easily, accommodate different topologies and protocols, and meet network throughput. The transmission mediums must support data rates based on network throughput, response time, and bit error rate requirements. Finally, the DELNET should include a fiber optic link for research uses. System software requirements were more rigorously developed using several SAT's (11:29-30). Since this investigation is limited to UNID hardware components, the reader is referred to other investigations for a complete development of DELNET software (11,9,10). The software developed for this investigation was only that necessary to perform a component test.

DELNET Design Summary

Topology, hosts, nodes, and transmission mediums were specified in the DELNET hardware design (11). The topology selected is shown in Fig 2-1. The basic ring architecture is a simple version of the local network proposed in the 1980 EEG report (28). The star topology for the local side of the network was chosen for three reasons (11:85-86). This arrangement decreases the number of nodes required, making each node more cost effective. The topology [illegible] practical interface for both the simplest and [illegible] computers in the laboratory. Finally, the [illegible] interact with each other [illegible] node, [illegible] the network [illegible].

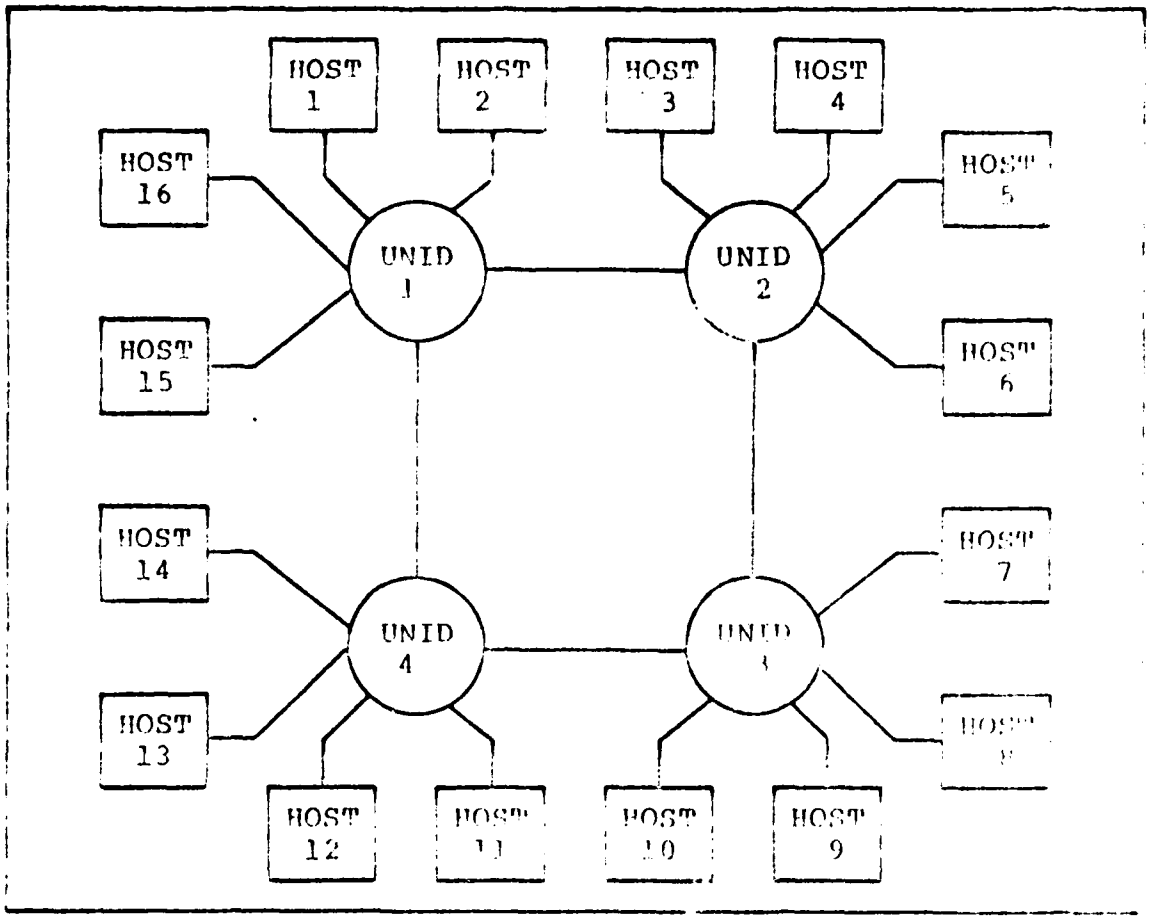

Fig 2-1 DELNET Topology.

Three hosts for the initial implementation were specified (11:86-87). These machines represented a minimum collection that would sufficiently exercise network protocols while providing the maximum resource sharing capabilities. The Vax-11/780 was chosen for its processing power and sophistication, and its capability to transfer files to and from the Cyber 750. The third series 11 Mac was chosen for its simplicity, high usage rate, and available [illegible] management system. The third, the Data General [illegible] chosen for its high usage rate, its link to the Data [illegible]

The node specified for the DELNET is the UNID (11:87-88). Currently available commercial nodes and networks are too expensive and not flexible enough for DELNET requirements. The UNID, however, offered several advantages. Complete documentation on development and design is available and non-proprietary. The use of two Z80 processors permits parallel processing, minimizing throughput and response time delays. Finally, a high level language, PL/Z, and a software development system, MCZ 1/25, are in place and available for further development.

The transmission medium selected for the DELNET includes both local and network channels (11:88-89). All local channels will use twisted pairs. One network link between two UNIDs will use a fiber optic communication channel.

Fig 2-2 shows the initial DELNET implementation with all the components discussed above.

UNID Design Summary

With the DELNET design complete, attention turned to the design of the UNID. The basic design of the device involves two Z80 microprocessor boards which share a 32K block of static RAM memory. Access to shared memory is through an arbitrator circuit (11:89) on the memory board. The UNID will interface to users directly and can interface with a communications network through local cards and network cards.

The local card provides the means to interface four RS-232C users with the device. Additional users are serviced by a UNID through the addition of a local card.

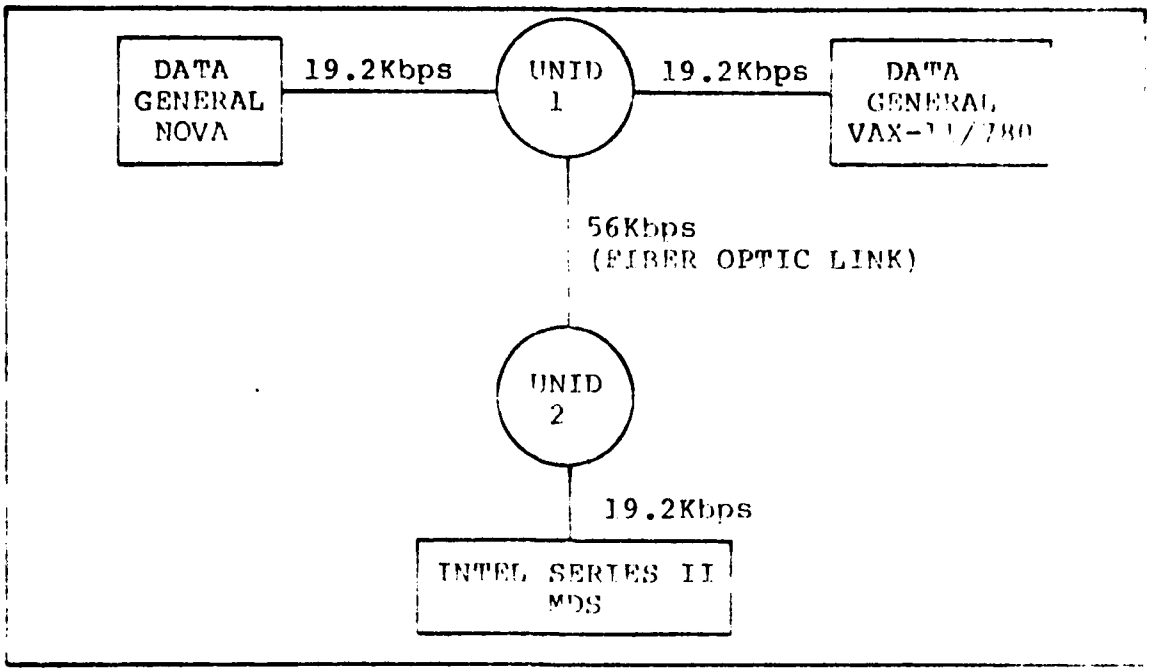

Fig 2-2 Proposed DELNET Configuration.

The network card was designed around the Z80-SIO, since the SIO provided significant capability for interfacing with different network protocols. Two network cards would be used in a device if the UNID was to act as an inter-ring interface mode. Fig 2-3 shows the block diagram of the UNID.

UNID Implementation.

Before a useable form of the DELNET could be built, at least two operational UNIDs were needed. These two, as shown in Fig 2-2, were used to form a least cost spanning tree (MST) network. In this case, the [illegible] simple ring network degenerates to a simple link between two nodes (20:171-174). Of course, more complex networks can be built by adding more links and nodes.

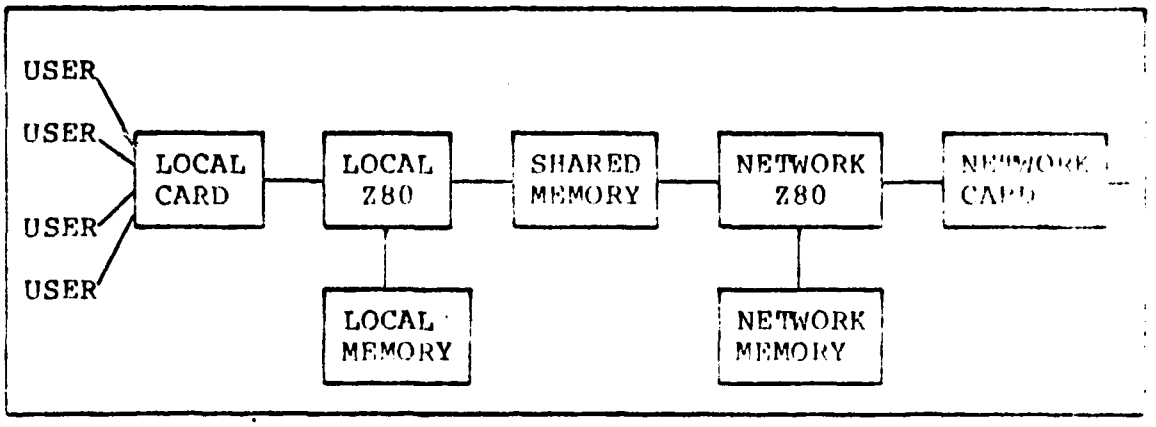

Fig 2-3 UNID Block Diagram.

shown in Fig 2-1. But, the MST approach requires a minimum of hardware to build a useable network.

A UNID prototype was completed by the end of 1980 (1). Since there was only one device, no numerical designation was assigned to it at that time. This device, however, did not meet the original design requirements. Specifically, UNID memory still needed to be expanded to 64K bytes and two additional I/O ports added. The next year saw these design requirements satisfied, a second UNID constructed (17), and numbers assigned. The first UNID built was designated UNID 1 and each of its cards were assigned the number 1, i.e. Local Card 1 and Network Processor 1. The second UNID completed was assigned the number 2, such as Network Processor 2 and Local Processor 2. The two UNIDs are identical to each other except in numerical designation. Their respective boards are interchangeable although an attempt is made to keep each UNIDs integrity. See Fig A-1, Motherboard Layout, for what cards and I/O ports are in a UNID system.

a simple network was formed, a few problem areas had to be eliminated. The numerous quantity of dynamic RAM chips used in the system memory produced transient signals caused by the continual refresh. This problem was corrected by using static RAM chips. This also eliminated the associated circuit coupling and switching noise due to the wire wraps. The details of these improvements are presented in chapter III.

Documentation

This ongoing investigation relies on proper documentation to provide a clear understanding of past work and future needs. Thus, an important part of this report was complete documentation of current hardware. The documentation includes various schematics, test results, layout charts, and wire wrap lists. This information is found in the Appendicies.

Summary

This chapter summarized the requirements and decisions for the UNID and DELNET. These represent the constraints placed on this investigation. These summaries were followed by the UNID and DELNET design implementation and evaluations conducted during this investigation.

III. UNID Implementation Modifications

This chapter details the implementation and modifications of the two UNIDs completed during this investigation. As mentioned earlier, there was no operable UNID available at the beginning of this thesis effort due to IC failures. The work accomplished to obtain such a UNID is discussed. Next, the design and construction of a system memory card is described. This led to the design and construction of two memory boards which consist of both system and shared memory. That work is described in this chapter.

Power Supply

Eventually, each UNID will be powered by a switching power supply, the Power/Mate ESM-200-4001, rated at [illegible] (18,17:27). One power supply was received; unfortunately, it had no power cables. An A/C power cord, connected through a switch, fuse, and indicator light was attached to the power supply. The four voltages (+5VDC,-5VDC,+12VDC,-12VDC) and ground were then connected to UNID 1. With the local monitor grounded, each time the power supply was turned on, the [illegible] would go to zero. It was determined that the power supply was switching intermittently. Therefore, it was returned and a replacement power supply ordered. In the meantime, the UNID was powered by a laboratory power supply. The [illegible] Electronics' Model M60-10-0V power supply was used for [illegible] since, it was the only available supply with [illegible]

capacity. The three-section Powertec Model 6C3000 power supply was used to supply the other three voltages.

The laboratory power supplies provided good regulation with essentially noise free power. An important feature of these two power supplies is their isolated DC grounds. The isolation prevents AC ripple and similar coupling interference reaching the UNID. All DC grounds were strapped together at the power supplies to further limit power supply interference. If different power supplies are substituted, care must be used to insure they are noise free and have isolated DC grounds. The replacement Power/Mate power supply was received; it was configured as the first and reconnected to a UNID.

UNID Update

At the start of this investigation, neither UNID was working on the local or the network side. Since each UNID components are interchangeable (although numbered as previously mentioned), an operable UNID was obtained using UNID 2 Motherboard, MCB Local Processor Card 1, Shared Memory Card 1 and Local Card 1. This UNID was only capable of filling and reading shared memory using a local monitor. It would not allow shared memory to be filled from the MCB due to an improper bit pattern being transmitted to the MCB when requesting a program transfer. The MCB indicated that data bit 2 was a constant high. That is, when requesting the transfer of program "[illegible]" the MCB received [illegible] and when requesting "[illegible]"

T.DEMO7. This was due to a failed data driver chip on the shared memory cards. One driver chip on each of the shared memory cards had failed. Replacement of these chips gave the UNID two operable shared memory cards when a local monitor was used.

After the defective shared memory cards were fixed, MCB Local Processor Card 1, Shared Memory Card 1, and Local Card 1 were placed into UNID 1 cage. This configuration worked properly.

When attempting to operate the MCB Network Processor cards with a network monitor, the local processor card was not installed. This was due to the fact that both processor boards were supposed to be identical. In this configuration, with only a network processor and shared memory card installed, the UNID would not work. This was because the network processor had its system clock disconnected and was using the local processors' clock routed through an inverter on the shared memory board. After this was discovered (shared memory card installed for network side to operate), the UNID had operable MCB Local and Network Processor cards, Shared Memory cards, and Local and Network cards.

Construction of the System Memory Card

System Memory Card 1 was constructed on a commercial Garry wire wrap card with certain modifications. [illegible] each board contained enough space for three 28-pin sockets, each system memory board [illegible] An extension for each [illegible]

edge. The IC sockets for the network portion of memory were installed and glued into place.

System memory, built from static RAM ICs, requires +5VDC and DC ground (8). The component surface of each board is connected to ground and physically connected to pin 8 of each 16-pin socket. Where a 14-pin socket was used, pin 8 was wire wrapped to pin 7 to provide ground. The wirewrap surface is likewise connected to +5VDC and connected to pin 16 of each 16-pin socket. The system memory card contained all control logic and memory ICs necessary for operation.

Design of the Memory Cards

After building and testing the new system memory board it was discovered that when the boundaries between processor, system, and shared memories were crossed, such as [illegible] memory from 1000(H) to FFFF(H), the system memory was unreliable. The reason was that the two separate memories (system and shared) used two different address decoders to select the individual memory chips. For this reason, it was decided to design a new memory board which would replace both the system memory board and the shared memory board and use the new 8K X 8 static RAM chips. The new design incorporated the control and logic of the former boards.

Construction of the Memory Cards

Memory cards 1 and 2 were constructed similar to the system memory card. All power requirements were [illegible] The only difference from the previous design [illegible] extension board [illegible] the rear of the [illegible]

large enough to hold seven memory ICs. Memory cards 1 and 2 function identical and are completely interchangeable.

The memory board was wire wrapped after the initial design of the memory card was completed and a working schematic was available. The first wire wrapped board did not work properly, as will be explained in Chapter IV, "Unit Testing." A second schematic was drawn based on board testing. Using this schematic (see Appendix B), a wire list program was generated and a second memory board was wire wrapped in accordance with this program. The program and wire list are shown in Appendix C. Based on the results of this second board testing and the wire list, the first memory board was disassembled and rewired.

The memory card contains all control logic and memory ICs necessary for operation. Appendix A shows the IC layout for the card. The top seven 28-pin chips are network system memory (2000(H) to 7FFF(H)) and shared memory (8000(H) to FFFF(H)). Below these are the three local system memory chips (2000(H) to 7FFF(H)). The rest of the chips on the board are for control.

Summary

This chapter provided a description of the [illegible] of the UNIT memory cards. The chapter also described [illegible] supply requirements. In Chapter IV, the design [illegible] hardware difficulties will be discussed in relation to the UNIT testing.

IV. UNID Testing

The final portion of this thesis investigation involved hardware testing the UNID and, in particular, the new memory cards. UNID testing was necessary in the beginning due to no operable system. UNID testing involved validation of wiring on the motherboards and all cards, functional logic tests, functional memory tests, and local card tests. The majority of the time was spent on testing the new memory cards. Hardware problems encountered are discussed along with their corrective actions. All testing was accomplished in accordance with previous theses (5,1,17).

UNID Testing Methods

The tests used to verify UNID operation were structured primarily as incremental bottom-up tests. This method was chosen for its several advantages in identifying errors. Once the initial components are checked, any new problems encountered are often caused by either an error in the newly added component or an error in the interaction with the new component. Also, the modularity of the UNID makes the incremental approach particularly attractive. Finally, most of the testing can be accomplished without complex involved hardware or software support.

The UNID circuit cards were used as the incremental component. Since most circuits were fully tested in previous theses (5,1,17), this investigation limited its testing to [illegible]

of card operation. At the outset of this investigation, there was no operable UNID. With this in mind and needing a starting point, all cards were first given a power-off check. The next tests were power-on checks without ICs. This was followed by power-on checks with ICs added. As each card passed its checks another card was added. The following sections describe each major area of testing and discuss the results.

Power-off Testing

Each board used in the UNID was checked for correct wiring. This check was accomplished when it was discovered that the UNID was not operating at the beginning of this investigation. Although these point-to-point wiring checks did not detect any wiring errors, they did ensure that power was not applied directly to ground and validated that signals were routed to the correct pins. This check also led to learning what signals were on each board and how they operated.

Very simple methods were used to validate wiring. In some cases, the wiring was visually checked. In cases where the wiring density was too great and a VOM had to be used to check continuity between pins.

Power-on Testing

The next series of tests were the power on tests of the installed chips. A VOM was used to verify the correct voltage at the proper pins.

The ICs were then installed and the cards were

UNID, adding one card at a time and checking it before the next card was added. Each card was checked for excessive heating when power was applied.

Functional Testing

Once the majority of wiring errors and faulty ICs were detected, each circuit card was tested to insure functional operation. The following sections describe this functional testing for each circuit card. The sequence of the following sections is the order in which the cards were tested.

Local Processor Card Testing

The local processor cards were functionally tested by installing them in the card cage, connecting the serial circuitry, and attaching an ATM-3 terminal as the local processor monitor terminal. These cards contained an EPROM monitor programmed during an earlier thesis (1). The board also contained 4K bytes of dynamic RAM. The functional testing involved resetting the processor card and exercising the various commands in the monitor (1:12-16). Proper operation of these commands was considered sufficient evidence that the processor was operating correctly. More stringent testing, such as attempting to move and load data, was accomplished as cards were added to the UNID and the processor tasks became more complex. For example, using the LOAD command with the local card installed not only tested the on-card memory, but also initialized the UNIBUS, established the priority interrupts, set the data block, etc. Each of these functions, executed by the local processor,

must perform correctly before a file can be loaded. Successfully loading data into memory was, therefore, taken as an indication that the local processor functioned properly.

Shared Memory Card Testing

The next cards tested were the shared memory cards. Each local monitor processor command was reinitiated, this time executing the commands within the boundaries of the memory on the shared memory cards. The shared memory was filled entirely with 00(H); then, the entire memory was displayed. This fill-display routine was repeated with different hexidecimal characters until all memory data bits were switched from zero to one to zero. Each time data bit was to be a zero, a one was displayed. This indicated to the data driver chips on the shared memory boards. chip driving the network side of shared memory had failed and was holding that bit high in memory. A similar problem encountered with both shared memory boards and [illegible] similarly. After replacing the chips, a block of [illegible] moved several times from one location to another within shared memory, then displayed. Finally, a single block [illegible] locations) of data within shared memory was [illegible] repeatedly. These three [illegible] tests were used [illegible] the basic operation and [illegible]

Network Processor Card Test[illegible]

After the local processor and shared memory [illegible] tested and operating, [illegible]

installed. As stated previously, this board was tested similarly to the local processor card. The only difference between the two cards is that the network processor card has no clock and needs the local processor card installed. A previous thesis discovered the local and network processor cards would operate together without interfering if the network clock was disabled, using instead the inverted clock from the local processor card (5:64-65). This inverted clock was obtained by wiring the clock signal from the local processor card through an inverter on the shared memory card and back to the clock circuit on the network processor card. With the proper boards installed, the terminal monitor described in the Local Processor Card Testing section was repeated for the network processor card. The memory fill-display routines in the Shared Memory Card Testing section were performed on the network processor card. Finally, the three cards were tested together. This was done by filling a portion of the local processor's on-card memory, moving that block into shared memory and then moving the same block into the network processor's on-card memory, using the network processor monitor. The entire test was then reversed, starting with the network processor's on-card memory and ending with the local processor's on-card memory. The sequence was repeated using several data patterns and different memory locations.

Local Card Testing

The local card was added to the UNID when the above series of tests were completed. A data file on disk on the MCZ was attempted to be loaded into the UNID through [illegible] Channel 1 using the load command. The file was unable to load due to the shared memory card's IC failures as related in Chapter III, UNID Update. After correcting the problem, the file's contents and location were validated visually.

System Memory Card Testing

The testing of this board was accomplished as outlined in the beginning of this chapter. The problem of unreliable data due to boundary crossing has been discussed in Chapter III. This led to the design of a combined memory board.

Memory Card Testing

The memory card would not operate properly when [illegible] after construction. Basically, three different [illegible] problems were found on this card: faulty design, fault[illegible], and timing faults. Each type of problem and its solution will be discussed in the following sections.

Design Faults

The Memory card was originally designed to [illegible] common address lines [illegible] shared memory, and network system memory. An arbiter chip was selected by a previous [illegible] to resolve [illegible] between the local and [illegible] memory. This circuit [illegible] to the [illegible]

$\overline{XSEL}$ and a $\overline{YSEL}$ depending on which processor $\overline{MREQ}$ signal arrived first. The present investigation NORed XA12, XA14, and XA15 together and NORed YA13, YA14, and YA15 together (see Fig B-2). This was accomplished to create an $\overline{XSEL}$ or $\overline{YSEL}$ whenever a memory location of 2000(H) and above was selected either on the local side or the network side. The $\overline{XSEL}$ and $\overline{YSEL}$ signals are used to enable the address line multiplexers. The $\overline{XMREQ}$ and $\overline{YMREQ}$ were used to select the data line bi-directional bus drivers.

The local system memory portion of the memory board was completed first and tested in accordance with previously discussed testing methods. This portion of the board passed all tests. The next portion of the board to be completed was shared memory. When this portion was tested, it was discovered that both the local system and shared memory bus drivers were being enabled at the same time when trying to read local system memory. This was causing a conflict on the data lines. To alleviate this problem, first, the [illegible] lines were separated so that each section (local, network and shared) had its own dedicated lines. Then $\overline{YSEL}$ and $\overline{XSEL}$ were each NANDed with $\overline{YSEL}$ and $\overline{XSEL}$, respectively, so that the network and local shared data bus drivers were selected if shared memory was not selected. This caused the local system and shared memory portions to work [illegible]. After the network portion was completed, it was found that both the network and local system memory were selected while trying [illegible].

because the same chip select line ($\overline{CE\text{-}XY2000}$, $\overline{CE\text{-}XY4000}$ and $\overline{CE\text{-}XY6000}$) was being used to enable each data bus driver. The only difference between the two was that each had its own read and write signals ($\overline{XRD}$, $\overline{XWR}$, $\overline{YRD}$, $\overline{YWR}$) for DIEN (Data In Enable Direction control). To correct this problem, the three chip select lines were NANDed together to create one chip select signal, $\overline{CE\text{-}XY}$, which was then NANDed with either $\overline{XSEL}$ or $\overline{YSEL}$ depending on which portion of the board was addressed. Now the individual portions of the memory card worked correctly.

Integrated Circuit Faults

An IC fault occurs if a chip fails to perform according to its truth table or specified function. Typically, a stuck fault, where the output remains high under all conditions, is corrected easily. The chip is simply removed and replaced. A fault where the output remains low under all conditions is more difficult to identify. A low condition fault may be caused by an internal short, an external short, or an internal short in the next stage. One effective way to determine an IC fault involves removing and replacing chips. A suspected faulty IC is removed and replaced by a known operable IC. If the circuit then works correctly, the suspect IC was probably the cause of the fault. If the circuit still works incorrectly, then the chip is returned to its place and another IC in the circuit is removed and replaced. [illegible] are found to be faulty [illegible]

wiring.

After redesigning the data bus drivers of the system memories, it was discovered that when the local monitor was used to fill shared memory with 00(H) and read, it displayed 00(H); but, when the network monitor was used to fill shared memory with 00(H) and read, it displayed 40(H). Data line DQ6 (pin 18) of the shared memory chips was only high when filled by the network monitor. When the network shared memory data bus drivers were removed, the shared memory worked fine. These two chips were then reversed and returned to their sockets. The result, when again filling with 00(H), was a displayed 04(H). The original data bus driver for line DQ6 was replaced with a good chip and the circuit functioned correctly.

While testing the new memory board, the local processor card failed. The only indication was that the local monitor would not reset. After checking the address lines and their associated chips, the data lines and their associated chips, and the EPROMs, it was discovered that one of the EPROMs had failed. This discovery was made by replacement with known good chips. The problem was not eliminated. A logic analyzer, in the memory map mode, attached to the CPU's address lines showed that the monitor program in the EPROMs was randomly addressing all of memory instead of remain in a tight loop waiting for an interrupt. This indication led to the stack pointer. The memory location of the stack point is resident in RAM, so the memory chips were replaced one by one

to determine if they were causing the problem. These were the only chips on the board which had not been examined. One chip had failed. It was removed and replaced with a good memory chip and the processor board then worked properly.

Memory Timing Faults

After the above faults were detected and corrected, the new memory card still failed to operate properly. The network system memory and the shared memory each worked correctly, but, the local system memory did not. During fill and display memory operations, a set pattern of unchanged data always occurred. The local and network sides were designed and wired similarly, but the local side would not create a chip select to any of its memory chips. All wiring and chips were checked and found to be proper. A chip select was forced by routing the $\overline{\text{CE-XY2000}}$ signal to local memory chip G1. This allowed the chip to operate but resulted in the same design problem as before (local and network memory being selected at the same time). The forcing of a chip select signal to G1 by-passed the ORing of $\overline{\text{CE-XY2000}}$ and $\overline{\text{XSEL}}$. This indicated a timing problem. These two signals were routed not from their sources but from other pins of the same signals. To ease the timing problem, the two signals were routed to the OR gate from their respective sources. This helped, but some unreliability in memory remained. A faster OR gate chip (74S32) was then used and the circuit worked perfectly.

UNID Testing

Once the memory card was found to be working by performing the simple monitor commands, a test program (L.VINT) was loaded into local system memory from the MCZ and run successfully. Then, the same program was moved into network system memory and run successfully. When this program was attempted to run in both local and network system memories simultaneously, only one side would run. Whichever memory (local or network) was started first would run until the other was started and then the first would stop. Not only would it stop, but the contents of its memory locations would be changed. Also, while running this program on the network side, the local side was loaded again from the MCZ. Loading caused noise interference to occur on the network monitor, and when the network side was then stopped and attempted to be restarted, it would not run.

At this point all checks were again run on the memory card and no errors were detected. This board was wire wrapped in accordance with the original design schematic. According to that diagram and the wiring of the board, the local and network sides were completely independent and showed no reason for interference. From the schematic a wire list program was completed which gave the signals at each pin and the routing of all wires. The board was then compared to the wire list and no discrepancies were detected. Since there seemed to be no differences between the board, the schematic, and the wire listing, and no faulty ICs could be

detected, it was decided to go ahead and construct a second memory card in accordance with only the wire list program. When this second board was completed and tested it also had a timing problem as mentioned earlier. The problem was corrected with the previously stated modification to the wire list (see Appendix C). The same program was then loaded into both sides of this board and attempted to run simultaneously. No interference was discovered and both sides ran independently. The first memory board constructed was then rewrapped in accordance with the wire list. Then, it was tested, as previously stated, and found to operate properly.

Chapter Summary

This chapter describes the testing performed on the UNID. The testing scheme chosen was organized from the bottom-up and followed the procedures of previous theses (1,5,17). The type of tests used were power-off, power-on, and functional tests. Also discussed were types of circuit problems encountered and solutions to the same.

V. Summary and Recommendations

The objective of this investigation was the continuation of the development of two message processors (UNIDs). This involved the designing, constructing, and testing of a new memory card. The software used in this thesis investigation either existed or was developed by a co-investigator (10). This chapter summarizes the results of this effort and suggests areas for further study.

Unid Completion

When this investigation began, two UNIDs were complete but neither was working. During this investigation, the two prototypes were tested for faulty wiring and ICs. All discrepancies found were corrected to produce two operable UNIDs. Completing the UNIDs required that a new memory card be constructed incorporating the circuitry of local and network system memories, and shared memory. The memory card was built using new technology, 8K X 8, static RAM chips. These memory chips allowed all 80K of memory to be built using only 10 memory chips and 33 control and logic chips.

UNID Testing

Each UNID was tested using an incremental bottom-up routine. Most of the UNID testing was limited to detecting IC faults inherited from previous theses. The remainder of the time was spent on testing the new memory card. Functional testing of this card revealed serious design

errors. These errors were finally corrected and two operable UNIDs are now in effect.

Recommendations

These recommendations include suggestions from past theses and involve further hardware development for the UNID and DELNET. Implementation of the Z80A processor is still a requirement of the original design. This involves replacing each Z80 MCB with the faster Z80A board. Unfortunately, Zilog no longer produces a Z80A MCB board. So, to upgrade the UNID a processor board would have to be designed and wire wrapped incorporating the Z80A CPU and associated circuitry. If a new processor board was designed and constructed it would be able to use the new static RAM chips and eliminate the dynamic RAMs now used on the MCB boards.

Also for future investigation is the use of a new Zilog 8-bit micro-processor chip which should be available in 1984 (25). This Z8108 has a multiplexed address and data bus to reduce the package pin count without sacrificing performance (memory transactions still require only three clock cycles). In addition, design with the Z8108 would be easy because of the on-chip oscillator and programmable bus timing features. The only external element required in the oscillator circuit is a crystal (whose frequency is twice the desired internal frequency). This chip can operate at speeds of 6 to 25 MHz for increased throughput. The programmable bus timing feature increases system throughput. Control-bit settings allow the internal processor clock to be scaled for external

bus accesses and wait states to be automatically inserted during bus cycles. Consequently, the user can select very high clock speeds to increase system performance without requiring high-speed memories and I/O devices.

Another recommendation deals with the network card. The original design goal for the network data rate is 1.5 Mbps. The Z80A-SIO can function at 880 Kbps in half duplex mode. The desired rate could be reached using the Signetic's 2652 Multi-protocol Communication Controller (MPCC) (20). The MPCC data rate is 2 Mbps and contains all Z80A-SIO features. It can also interface with an 8-bit or 16-bit data bus. Thus, this addition would be compatible with 16-bit message processors.

Now that there are two operable UNIDs having reliable static memories, future investigations will be able to concentrate more on the development of the DELNET rather then the hardware of the UNID.

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APPENDIX A

CIRCUIT CARD LAYOUTS

This appendix contains a collection of diagrams illustrating the IC layout for three circuit cards used in the UNID, including the motherboard. The local and network processor cards are not included here, but are well documented in the Z80 MCB User's Manual (27).

List of Figures

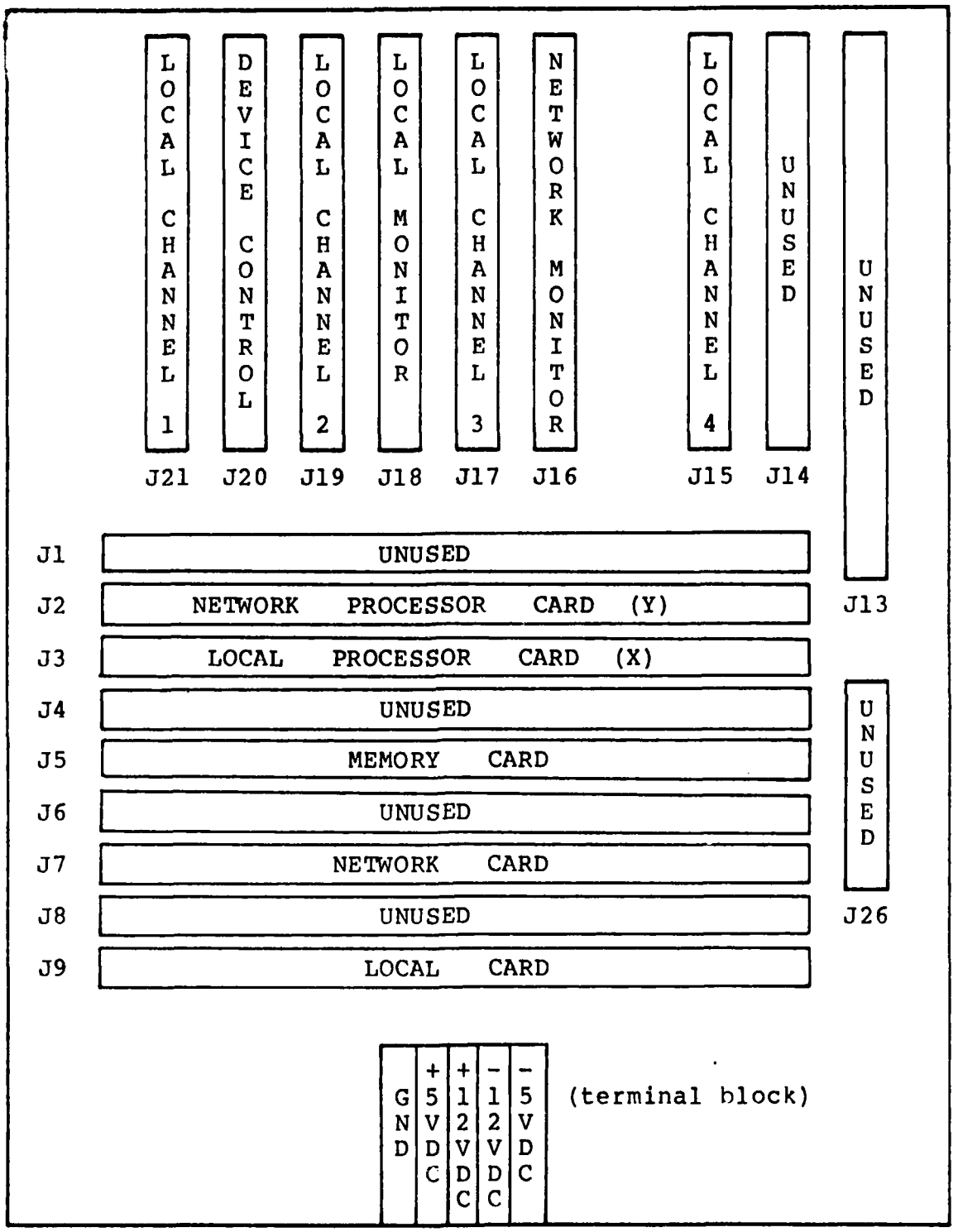


Fig A-1 Motherboard Layout.

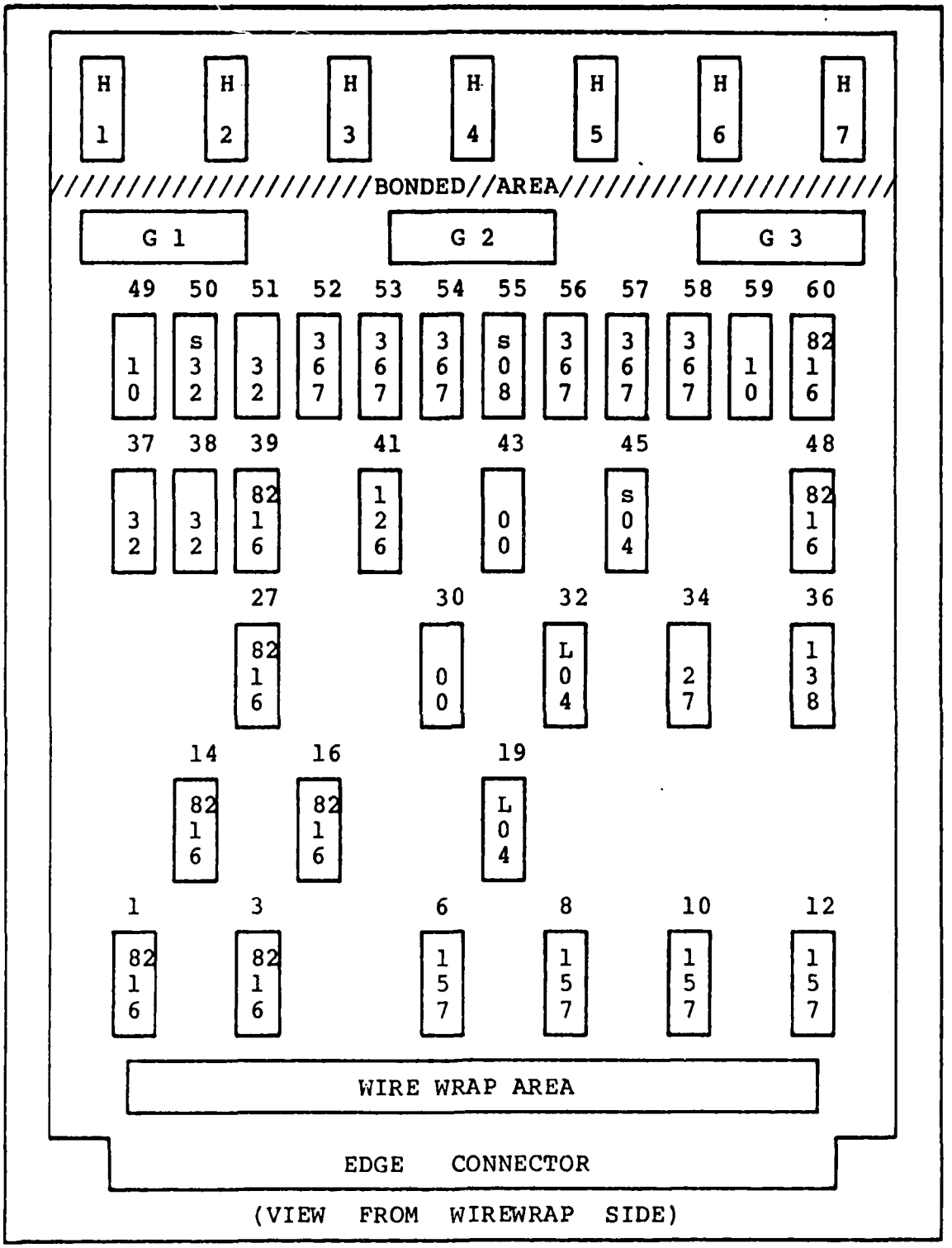
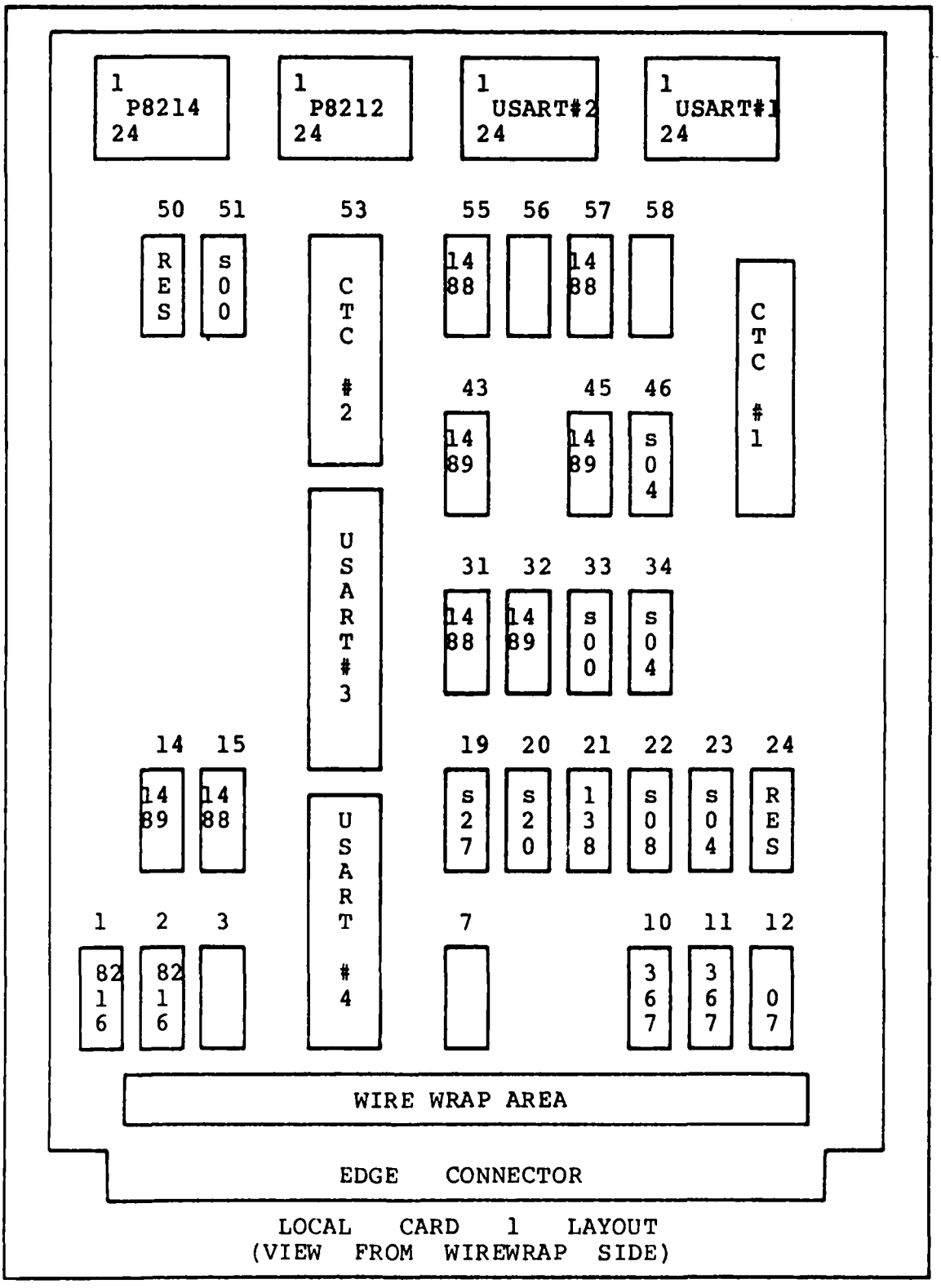


Fig A-2 Memory Card Layout.



LOCAL CARD 1 LAYOUT
(VIEW FROM WIREWRAP SIDE)

Fig A-3 Local Card 1 Layout.

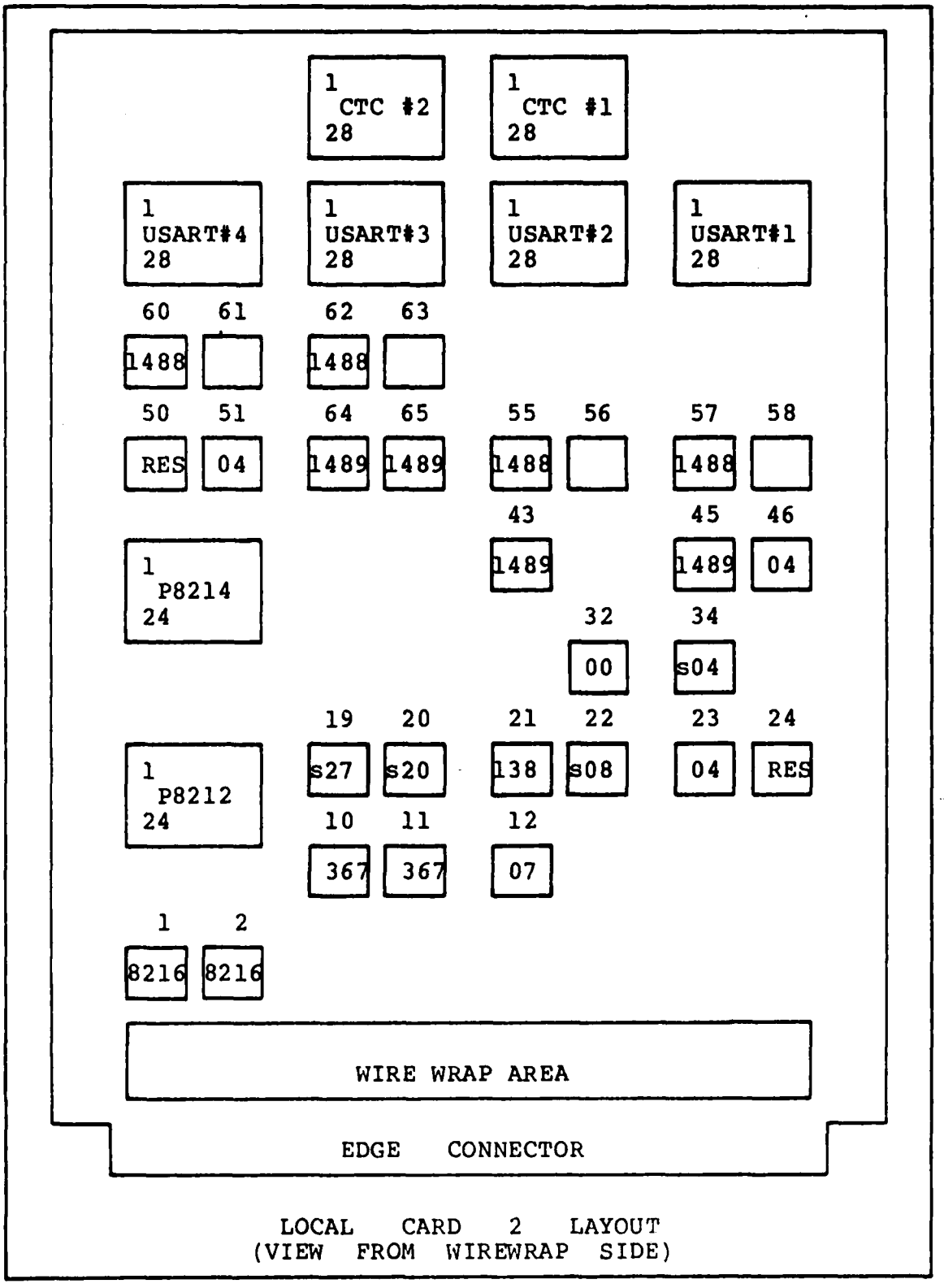


Fig A-4 Local Card 2 Layout.

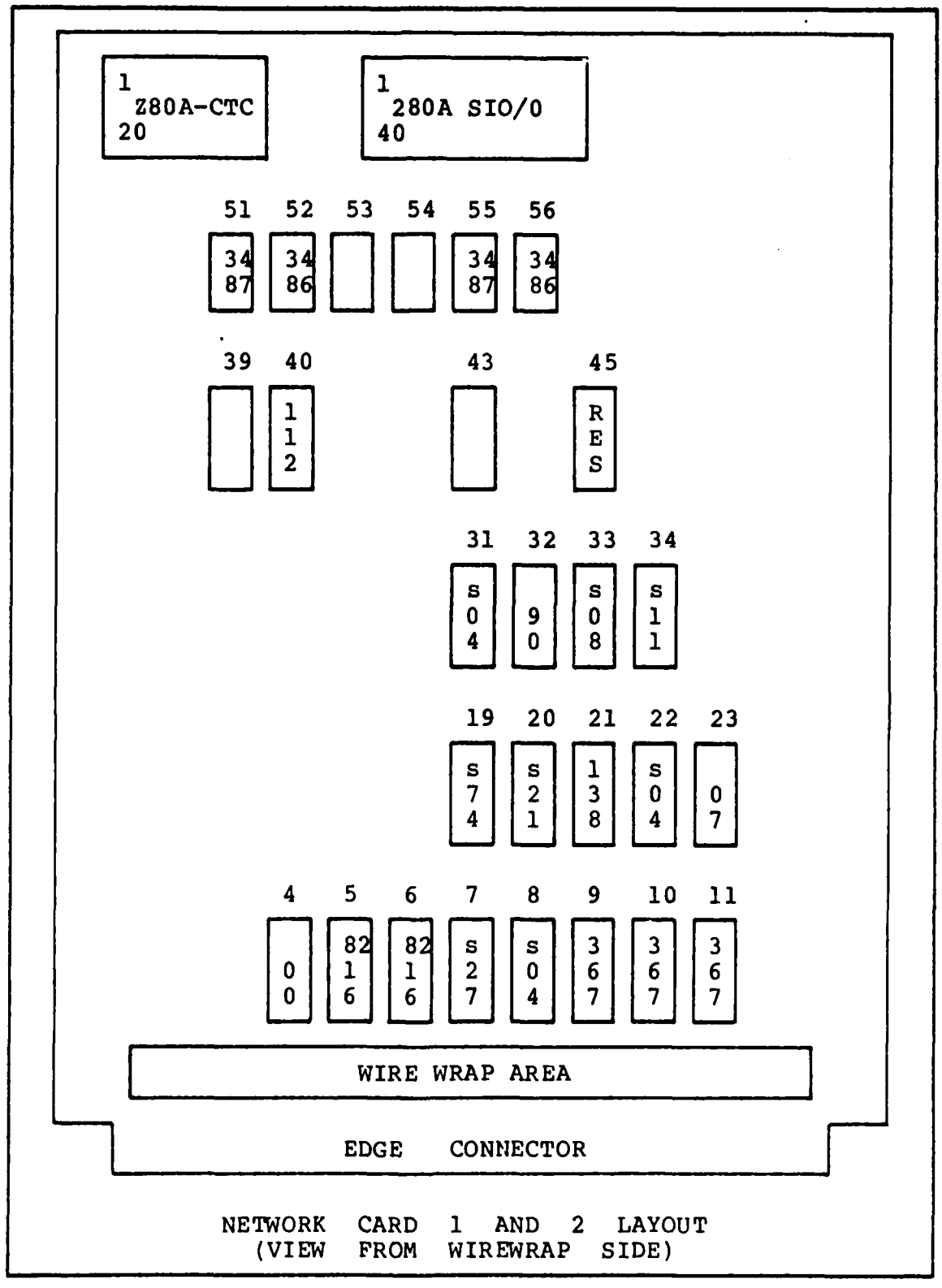


Fig A-5 Network Card Layout.

Appendix B

Circuit Card Schematics

This appendix contains the circuit schematics for three of the UNID circuit cards, including the motherboard. The circuit schematics for the local processor and network processor cards are contained in the Z80 MCB User's Manual (27).

List of Figures

This figure lists the wiring connections made on the motherboard of UNIDs 1 and 2. The head of each column corresponds to a connector on the motherboard. The verticle column at the left of the figure lists the particular signals being described. The numbers in the figure represent the wire wrap pin numbers where the signal is attached to the given connector. All signals on the motherboard are grouped according to function.

	J2	J3	J5	J7	J9	J15	J16	J17	J18	J19	J20	J21
LOCAL PROCESSOR ADDRESS BUS (X)												
XA0	*	103	90	*	103	*	*	*	*	*	*	*
XA1	*	102	92	*	102	*	*	*	*	*	*	*
XA2	*	101	94	*	101	*	*	*	*	*	*	*
XA3	*	100	96	*	100	*	*	*	*	*	*	*
XA4	*	98	91	*	98	*	*	*	*	*	*	*
XA5	*	29	93	*	29	*	*	*	*	*	*	*
XA6	*	30	95	*	30	*	*	*	*	*	*	*
XA7	*	26	97	*	26	*	*	*	*	*	*	*
XA8	*	27	29	*	27	*	*	*	*	*	*	*
XA9	*	89	31	*	89	*	*	*	*	*	*	*
XA10	*	91	33	*	91	*	*	*	*	*	*	*
XA11	*	37	35	*	37	*	*	*	*	*	*	*
XA12	*	97	30	*	97	*	*	*	*	*	*	*
XA13	*	36	32	*	36	*	*	*	*	*	*	*
XA14	*	94	34	*	94	*	*	*	*	*	*	*
XA15	*	32	36	*	32	*	*	*	*	*	*	*
LOCAL PROCESSOR DATA BUS (X)												
XD0	*	13	68	*	13	*	*	*	*	*	*	*
XD1	*	75	69	*	75	*	*	*	*	*	*	*
XD2	*	71	7	*	71	*	*	*	*	*	*	*
XD3	*	8	8	*	8	*	*	*	*	*	*	*
XD4	*	68	70	*	68	*	*	*	*	*	*	*
XD5	*	5	71	*	5	*	*	*	*	*	*	*
XD6	*	12	9	*	12	*	*	*	*	*	*	*
XD7	*	73	10	*	73	*	*	*	*	*	*	*

Fig B-1 Motherboard Wiring List.

	J2	J3	J5	J7	J9	J15	J16	J17	J18	J19	J20	J21
LOCAL PROCESSOR CONTROL SIGNALS (X)												
XWR	*	23	117	*	23	*	*	*	*	*	*	*
XRFSH	*	35	*	*	*	*	*	*	*	*	*	*
XRD	*	116	111	*	116	*	*	*	*	*	*	*
XM1	*	115	*	*	115	*	*	*	*	*	*	*
XMREQ	*	85	110	*	*	*	*	*	*	*	*	*
XIORQ	*	4	*	*	4	*	*	*	*	*	*	*
XWAIT	*	119	55	*	*	*	*	*	*	*	*	*
XINT	*	79	*	*	79	*	*	*	*	*	*	*
XRESET	*	10	*	*	31	*	*	*	*	*	5	*
XCLK	39	99	*	*	99	*	*	*	*	*	*	*
XCLK/2	*	118	56	*	*	*	*	*	*	*	*	*
LOCAL PROCESSOR MONITOR CHANNEL (X)												
XTxD	*	15	*	*	*	*	*	*	2	*	*	*
XRxD	*	7	*	*	*	*	*	*	3	*	*	*
XRTS	*	14	*	*	*	*	*	*	4	*	*	*
XCTS	*	11	*	*	*	*	*	*	5	*	*	*
XDSR	*	74	*	*	*	*	*	*	6	*	*	*
XGND	*	64	*	*	*	*	*	*	7	*	*	*
XLSD	*	80	*	*	*	*	*	*	8	*	*	*
XDTR	*	76	*	*	*	*	*	*	20	*	*	*
NETWORK PROCESSOR ADDRESS BUS (Y)												
YA0	103	*	100	103	*	*	*	*	*	*	*	*
YA1	102	*	102	102	*	*	*	*	*	*	*	*
YA2	101	*	104	101	*	*	*	*	*	*	*	*
YA3	100	*	106	100	*	*	*	*	*	*	*	*
YA4	98	*	101	98	*	*	*	*	*	*	*	*
YA5	29	*	103	29	*	*	*	*	*	*	*	*
YA6	30	*	105	30	*	*	*	*	*	*	*	*
YA7	26	*	107	26	*	*	*	*	*	*	*	*
YA8	27	*	39	*	*	*	*	*	*	*	*	*
YA9	89	*	41	*	*	*	*	*	*	*	*	*
YA10	91	*	43	*	*	*	*	*	*	*	*	*
YA11	37	*	45	*	*	*	*	*	*	*	*	*
YA12	97	*	40	*	*	*	*	*	*	*	*	*
YA13	36	*	42	*	*	*	*	*	*	*	*	*
YA14	94	*	44	*	*	*	*	*	*	*	*	*
YA15	32	*	46	*	*	*	*	*	*	*	*	*
NETWORK PROCESSOR DATA BUS (Y)												
YD0	13	*	74	13	*	*	*	*	*	*	*	*
YD1	75	*	75	75	*	*	*	*	*	*	*	*

Fig B-1 Motherboard Wiring List (cont).

	J2	J3	J5	J7	J9	J15	J16	J17	J18	J19	J20	J21
YD2	71	*	13	71	*	*	*	*	*	*	*	*
YD3	8	*	14	8	*	*	*	*	*	*	*	*
YD4	68	*	76	68	*	*	*	*	*	*	*	*
YD5	5	*	77	5	*	*	*	*	*	*	*	*
YD6	12	*	15	12	*	*	*	*	*	*	*	*
YD7	73	*	16	73	*	*	*	*	*	*	*	*
NETWORK PROCESSOR CONTROL SIGNALS (Y)												
YWR	23	*	119	23	*	*	*	*	*	*	*	*
YRFSH	35	*	*	*	*	*	*	*	*	*	*	*
YRD	116	*	113	116	*	*	*	*	*	*	*	*
YWAIT	119	*	57	119	*	*	*	*	*	*	*	*
YM1	115	*	*	115	*	*	*	*	*	*	*	*
YMRQ	85	*	112	85	*	*	*	*	*	*	*	*
YIORQ	4	*	*	4	*	*	*	*	*	*	*	*
YINT	79	*	*	79	*	*	*	*	*	*	*	*
YRESET	10	*	*	31	*	*	*	*	*	*	10	*
YCLK	99	*	*	99	*	*	*	*	*	*	*	*
YCLK/2	118	*	58	*	*	*	*	*	*	*	*	*
NETWORK PROCESSOR MONITOR CHANNEL (Y)												
YTxD	15	*	*	*	*	*	2	*	*	*	*	*
YRxD	7	*	*	*	*	*	3	*	*	*	*	*
YRTS	14	*	*	*	*	*	4	*	*	*	*	*
YCTS	11	*	*	*	*	*	5	*	*	*	*	*
YDSR	74	*	*	*	*	*	6	*	*	*	*	*
YGND	64	*	*	*	*	*	7	*	*	*	*	*
YLSD	80	*	*	*	*	*	8	*	*	*	*	*
YDTR	76	*	*	*	*	*	20	*	*	*	*	*
LOCAL CHANNEL 1												
TxD	*	*	*	*	57	*	*	*	*	*	*	2
RxD	*	*	*	*	58	*	*	*	*	*	*	3
RTS	*	*	*	*	52	*	*	*	*	*	*	4
CTS	*	*	*	*	53	*	*	*	*	*	*	5
DSR	*	*	*	*	54	*	*	*	*	*	*	6
LSD	*	*	*	*	56	*	*	*	*	*	*	8
DTR	*	*	*	*	55	*	*	*	*	*	*	20
LOCAL CHANNEL 2												
TxD	*	*	*	*	49	*	*	*	*	2	*	*
RxD	*	*	*	*	50	*	*	*	*	3	*	*
RTS	*	*	*	*	44	*	*	*	*	4	*	*
CTS	*	*	*	*	45	*	*	*	*	5	*	*

Fig B-1 Motherboard Wiring List (cont).

	J2	J3	J5	J7	J9	J15	J16	J17	J18	J19	J20	J21
DSR	*	*	*	*	46	*	*	*	*	6	*	*
LSD	*	*	*	*	48	*	*	*	*	8	*	*
DTR	*	*	*	*	47	*	*	*	*	20	*	*
LOCAL CHANNEL 3												
TxD	*	*	*	*	37	*	*	2	*	*	*	*
RxD	*	*	*	*	38	*	*	3	*	*	*	*
RTS	*	*	*	*	32	*	*	4	*	*	*	*
CTS	*	*	*	*	33	*	*	5	*	*	*	*
DSR	*	*	*	*	34	*	*	6	*	*	*	*
LSD	*	*	*	*	36	*	*	8	*	*	*	*
DTR	*	*	*	*	35	*	*	20	*	*	*	*
LOCAL CHANNEL 4												
TxD	*	*	*	*	19	2	*	*	*	*	*	*
RxD	*	*	*	*	20	3	*	*	*	*	*	*
RTS	*	*	*	*	14	4	*	*	*	*	*	*
CTS	*	*	*	*	15	5	*	*	*	*	*	*
DSR	*	*	*	*	16	6	*	*	*	*	*	*
LSD	*	*	*	*	18	8	*	*	*	*	*	*
DTR	*	*	*	*	17	20	*	*	*	*	*	*

Fig B-1 Motherboard Wiring List (cont).

In addition to the wiring connections listed above, each MCB processor card has a number of jumper connections on its edge connector. See the Z80 MCB User's Manual (27) for further information.

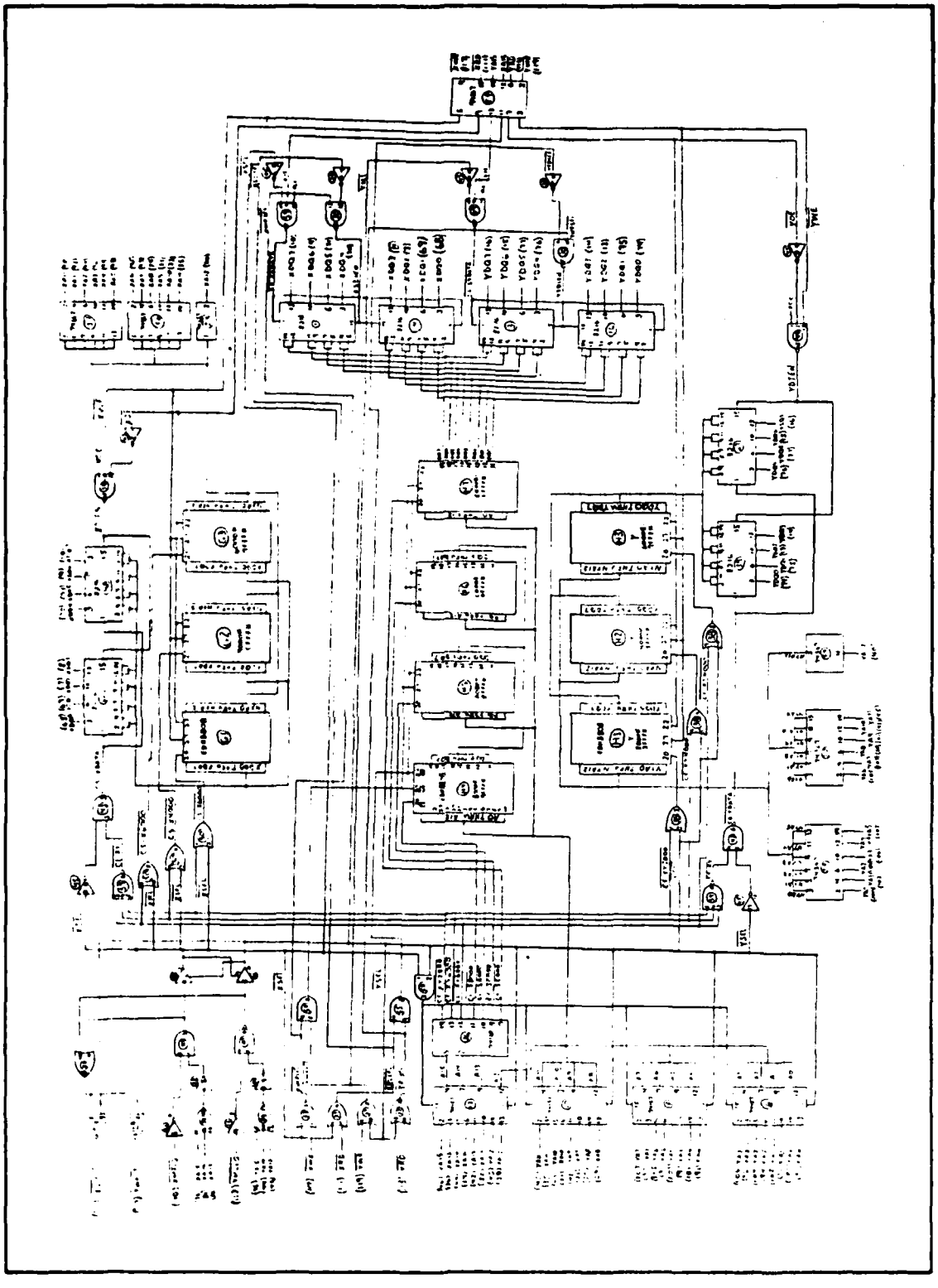


Fig B-2 Memory Card Schematic.

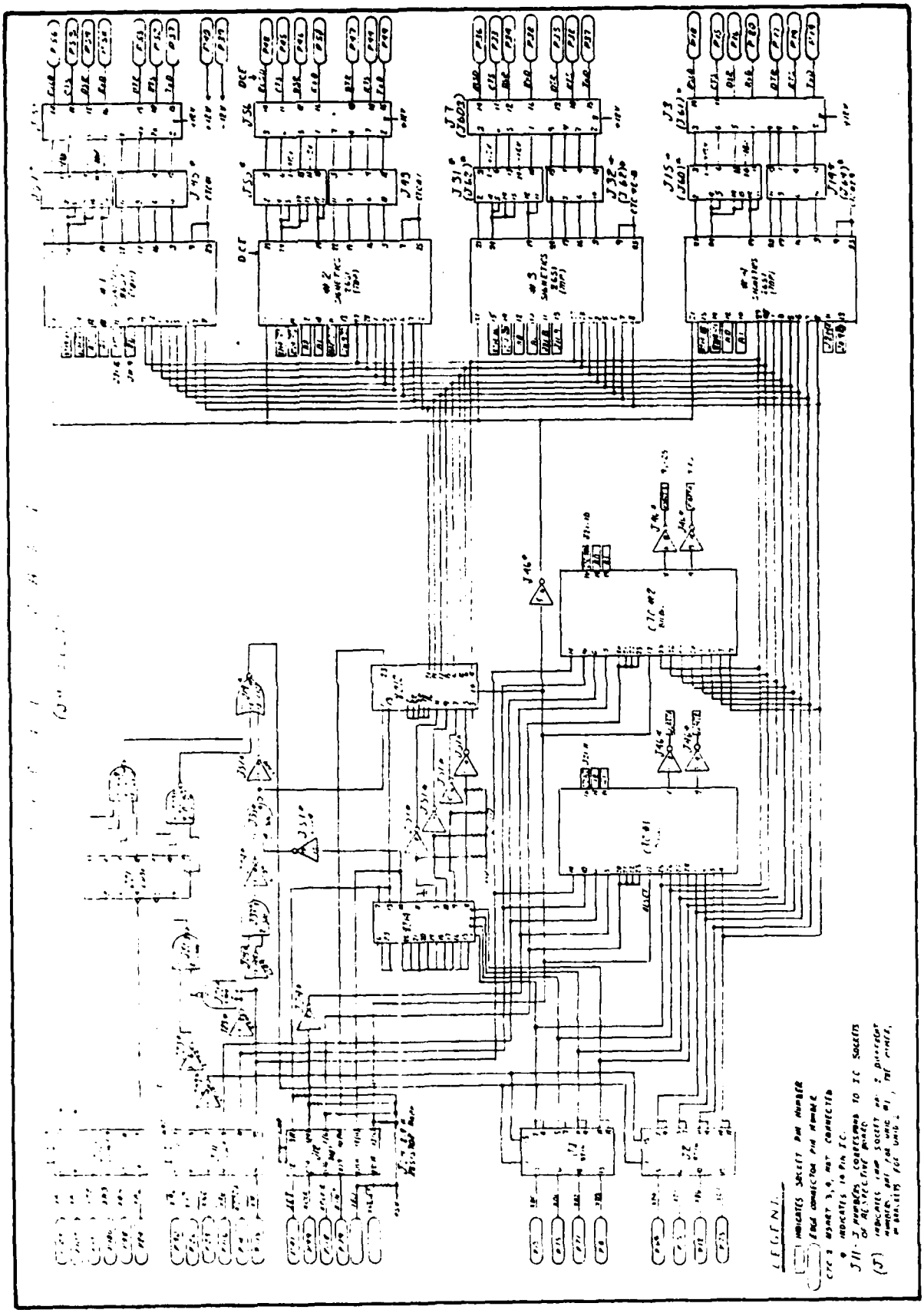


Fig B-3 Local Card Schematic.

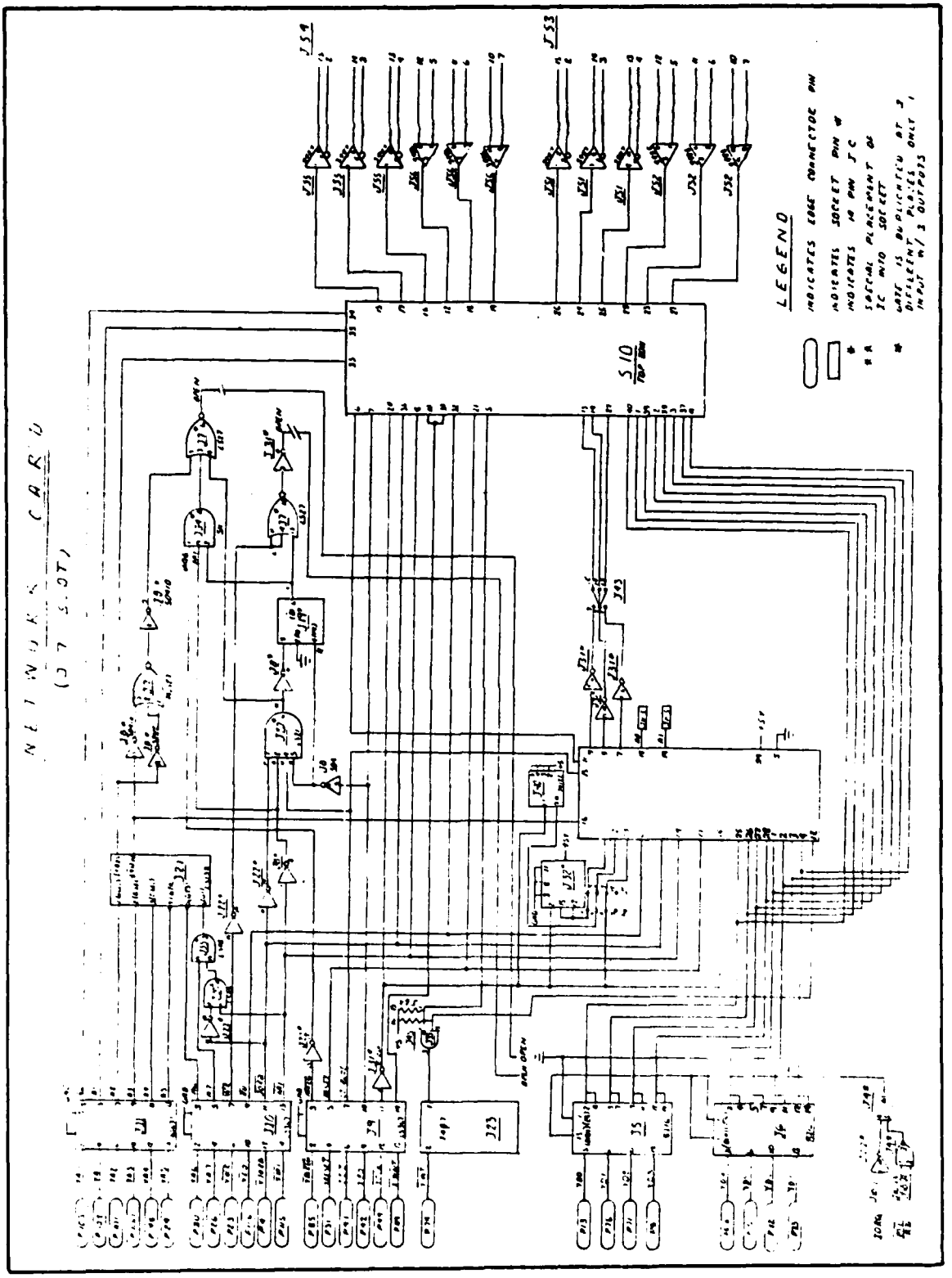


Fig B-4 Network Card Schematic.

Appendix C

Wiring List Program

This appendix contains the wire list users manual which was used to generate the wire routing program included at the end of this appendix. The card deck which must be loaded into the CDC computer may be obtained from Dr. Lamont, AFIT/ENG. That program must be loaded before the users' program can be run.

Contents

WLIST USERS MANUAL

I. General Description

The purpose of WLIST is to aid the hardware designer in generating an error free wire list, provide a part of the standard documentation of hardware design, and allow much simplified updating of documentation after a change in design has been made.

How It Works - The user provides a list of signal connections to each IC, plug, jack or other similar device. The data is sorted and collated in several different ways to provide the various output formats. An approximation of the best sequence of connections for each signal is generated. Errors of certain types can be detected and diagnostic messages are issued.

Output Forms - There are three output products. The first is essentially a reformatting of the input data. By unit (IC, etc.), the pin numbers and signals connected are listed. The second product is a list of all unit/pin connections by signal name, starting with the source of the signal. Also listed is the fan-out of each signal. The third product is a connection by connection wiring list, with separate lists for each level of wire wrap.

II. How to Use the Program

Input Cards - There are three types of data card: 1) the title card, 2) unit cards, and 3) connection cards.

The title card contains an asterisk followed by a title of up to 20 characters. The title is printed on each page of the output listing.

example *PROM BOARD

Unit cards contain the location, number of pins, and name (or comment) of each IC, connector, etc., on the board. One unit card is required per device. The first character is a dollar sign; followed by location (e.g. A:4), number of pins (1-999) and up to 10 comment characters.

example $A:4,24,EPROM 2708

Connection cards contain the names of signals to be connected to each pin of a device defined by a unit card. As many connection cards as necessary follow each unit card. Signal names of up to 10 characters are listed, separated by commas, starting with pin 1. Pins intended to have no connection must be named "NC". One signal source must be specified for each signal name used on a board. The source is identified by an asterisk preceeding the signal name. Connection cards may only use the first 72 columns. Columns 73 through 80 are reserved for optional sequence numbers.

example $D:8,14,AND 7408
ENA1,CLK,*STB1,ENA2,CLK,*STB2,
GND,NC,NC,NC,NC,NC,NC,VCC

Executing the Program

WLIST can be run using a card reader or a time-sharing terminal.

If run using a card reader, the following control card deck should be used.

```
$JOB H80 SYST BCDDMP PRI=15 OUT=0
*RJE 100 H80 *
3 initials,T15,CM77000,IO20,.T820665,name,box #,phone #
ATTACH,WLIST,ID=E770050,SN=ASDEN,CY=1.
LIBRARY,COBOL.
COPY,INPUT,WLDATA.
REWIND,WLDATA,WLIST.
WLIST.
REWIND,WLDATA,WLIST.
7/8/9
data cards
6/7/8/9
```

See Fig C-1 for a sample card deck.

If executed from a time-sharing terminal, the "deck" should contain the same control cards used above, with "*EOR" substituted for "7/8/9" and "*EOF" substituted for "6/7/8/9".

III. Interpreting the Output

Two header pages are printed identifying the circuit, version of WLIST, and the date and time at which the job was run. This allows immediate identification of the most recent run.

The normal output is self-explanatory. Signal sources are identified by a leading asterisk. The wire list output is provided in wire wrap levels. All level one connections should be made prior to proceeding to level two. This will eliminate wiring level changes and make later modification of

```
$JOB H80 SYST BCDDMP PRI=15 OUT=0
*RJE 100 H80 *
GFC,T15,CM77000,IO20,.T820665,CUOMO,4093,55533
ATTACH,WLIST,ID=E770050,SN=ASDEN,CY=1.
LIBRARY,COBOL.
COPY,INPUT,WLDATA.
REWIND,WLDATA,WLIST.
WLIST.
REWIND,WLDATA,WLIST.
7/8/9
*WLIST EXAMPLE
$A:1,16,CNTR 74161
CLR,CLK,D4,D5,D6,D7,ENA,GND,
LD*,ENA,A0,A1,A2,A3,*C1,VCC
$B:1,16,CNTR 74161
CLR,CLK,D0,D1,D2,D3,C1,GND,
LD*,C1,A4,A5,A6,A7,*OVR,VCC
$C:1,25,CONNECTOR
*D0,*D1,*D2,*D3,*D4,*D5,*D6,*D7,*LD*,*ENA,*CLK,NC,
*VCC,*GND,*CLR,NC,*A0,*A1,*A2,*A3,*A4,*A5,*A6,*A7,OVR
6/7/8/9
```

Fig C-1 Example Card Deck.

the circuit easier. Since the algorithm for determining the sequence is a simple one, the results may not always be the best possible. If there are signals that are sensitive to excessive wire length, their routing should be checked before the board is wired. Space is provided on the wire list to enter information such as wire gauge and color or other appropriate remarks. The list is designed to be cut down to 8 x 10 1/2 size for easy use at the lab bench.

Error Diagnostics - A moderate amount of error checking is done in the program. As with all such error diagnostics, care must be used in interpretation because the actual error may not be exactly that indicated. The commonly encountered error messages will be discussed briefly.

If a signal name occurs only once, an informative diagnostic advises that the fan-out is zero. This may result from a typographic error in the string name.

If no source is declared for a signal, an informative diagnostic advises that there is no source. This may also indicate a typographic error.

If more than one source has been declared for a signal, an informative diagnostic advises such.

If an error has been detected, the wire list will be aborted and a fatal diagnostic will be printed. This is necessary because results of the wire list are unpredictable if errors have been encountered.

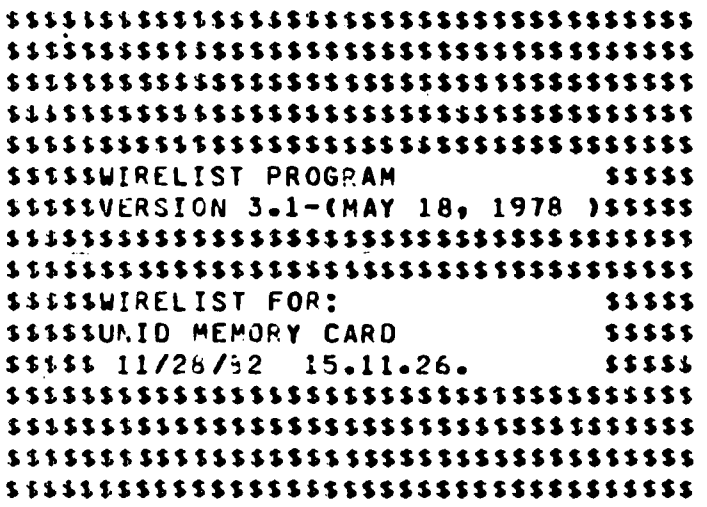
IV. Conclusion

Although it will probably be more work for the designer to generate a wire list with this program, it has been found that it is useful in removing errors from the wire list and, in some cases, pointing out design errors. It forces more discipline on the designer, particularly in the often neglected area of documentation. It is of particular advantage in keeping documentation up-to-date when changes are made in the design after fabrication. The few cards affected can be changed, the program rerun, and a completely new, up-to-date set of documentation, without penciled corrections, is available. If done properly, use of the program can be well worth the time.

WIRE ROUTE LISTING

Following is the wire routing listing which was used to wire wrap the new memory boards built for the UNIDs. On this page is listed a guide to the correlation between the list's chip locations and the card's chip socket labels.

A:1 = Edge Connector
B:1 = 1
B:13 = 3
B:16 = 6
B:18 = 8
B:21 = 10
B:23 = 12
C:12 = 14
C:14 = 16
C:17 = 19
D:13 = 27
D:16 = 30
D:18 = 32
D:21 = 34
D:23 = 36
E:11 = 37
E:12 = 38
E:13 = 39
E:15 = 41
E:17 = 43
E:19 = 45
E:23 = 48
F:11 = 49
F:12 = 50
F:13 = 51
F:14 = 52
F:15 = 53
F:16 = 54
F:17 = 55
F:18 = 56
F:19 = 57
F:21 = 58
F:22 = 59
F:23 = 60


WIRELIST PROGRAM
VERSION 3.1-(MAY 18, 1978)
WIRELIST FOR:
UNID MEMORY CARD
11/26/82 15.11.26.

```
UNIT C NNECTIONS FOR UNIX MEMORY CARD                                    PAGE   1
##########################################################################################
#A:1                                                                                     #
#EDGE PINS                                                                               #
# 1 NC          9*XDQ6        17 NC         25 NC         33*XA10       41*YA9          #
# 2 NC          10*XDQ7       18 NC         26 NC         34*XA14       42*YA13         #
# 3 NC          11 NC         19 NC         27 NC         35*XA11       43*YA10         #
# 4 NC          12 NC         20 NC         28 NC         36*XA15       44*YA14         #
# 5 NC          13*YDQ2       21 NC         29*XA8        37 NC         45*YA11         #
# 6 NC          14*YDQ3       22 NC         30*XA12       38 NC         46*YA15         #
# 7*XDQ2        15*YDQ6       23 NC         31*XA9        39*YA8        47 NC           #
# 8*XDQ3        16*YDQ7       24 NC         32*XA13       40*YA12       48 NC           #
##########################################################################################
#A:1                                                                                     #
#EDGE PINS                                                                               #
 49 NC          57 YWAIT      65 NC         73 NC         81 NC         89 NC           #
 50 NC          58 YCLK/2     66 NC         74*YDQ0       82 NC         90*XA0          #
 51 NC          59 NC         67 NC         75*YDQ1       83 NC         91*XA4          #
 52 NC          60*VCC        68*XDQ0       76*YDQ4       84 NC         92*XA1          #
 53 NC          61 NC         69*XDQ1       77*YDQ5       85 NC         93*XA5          #
 54 NC          62 NC         70*XDQ4       78 NC         86 NC         94*XA2          #
 55 XWAIT       63 NC         71*XDQ5       79 NC         87 NC         95*XA6          #
 56*XCLK/2      64 NC         72 NC         80 NC         88 NC         96*XA3          #
##########################################################################################
#A:1                                                     #B:11                           #
#EDGE PINS                                              ##216SXDATA                     #
 97*XA7        105*YA6       113*YWD       121 NC        # 1 CS-SXDATA   9*SDQ6          #
 98 NC         106*YA3       114 NC        122 NC        # 2*SDQ4        10 XDQ6         #
 99 NC         107*YA7       115 NC                      # 3 XDQ4        11 SDQ6         #
100*YA0        108 NC        116 NC                      # 4 SDQ4        12*SDQ7         #
101*YA4        109 NC        117*XWR                     # 5*SDQ5        13 XDQ7         #
102*YA1        110*XMREQ     118 NC                      # 6 XDQ5        14 SDQ7         #
103*YA5        111*XRD       119*YWR                     # 7 SDQ5        15 XSDIEN       #
104*YA2        112*YMREQ     120*GND                     # 8 GND         16 VCC          #
##########################################################################################
```

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#B:13		#B:16		#B:19	
#8216YDATA		#74157-6		#74157-8	
# 1 CS-SYDATA	9 SDQ6	# 1 YSEL	9*A1	# 1 YSEL	9*A5
# 2 SDQ4	10 YDQ6	# 2 YA3	10 XA1	# 2 YA7	10 XA5
# 3 YDQ4	11 SDQ6	# 3 XA3	11 YA1	# 3 XA7	11 YA5
# 4 SDQ4	12 SDQ7	# 4*A3	12*A0	# 4*A7	12*A4
# 5 SDQ5	13 YDQ7	# 5 YA2	13 XA0	# 5 YA6	13 XA4
# 6 YDQ5	14 SDQ7	# 6 XA2	14 YA0	# 6 XA6	14 YA4
# 7 SDQ5	15 YSDIEN	# 7*A2	15 STROBE	# 7*A6	15 STROBE
# 8 GND	16 VCC	# 8 GND	16 VCC	# 8 GND	16 VCC

#B:21		#B:23		#C:12	
#74157-10		#74157-12		#8216SYDATA	
# 1 YSEL	9*A9	# 1 YSEL	9*A13	# 1 CS-SXDATA	9*SDQ2
# 2 YA11	10 XA9	# 2 YA15	10 XA13	# 2*SDQ0	10 XDQ2
# 3 XA11	11 YA9	# 3 XA15	11 YA13	# 3 XDQ0	11 SDQ2
# 4*A11	12*A8	# 4*A15	12*A12	# 4 SDQ0	12*SDQ3
# 5 YA10	13 XA8	# 5 YA14	13 XA12	# 5*SDQ1	13 XDQ3
# 6 XA10	14 YA8	# 6 XA14	14 YA12	# 6 XDQ1	14 SDQ3
# 7*A10	15 STROBE	# 7*A14	15 STROBE	# 7 SDQ1	15 XSDIEN
# 8 GND	16 VCC	# 8 GND	16 VCC	# 8 GND	16 VCC

#C:14		#C:17		#D:13	
#8216YDATA		#74C4NOT19		#8216YDATA	
# 1 CS-SYDATA	9 SDQ2	# 1 NC	9 NC	# 1 CS-YDATA	9*NYDQ6
# 2 SDQ0	10 YDQ2	# 2 NC	10 NC	# 2*NYDQ4	10 YDQ6
# 3 YDQ0	11 SDQ2	# 3 NC	11 NC	# 3 YDQ4	11 NYDQ6
# 4 SDQ0	12 SDQ3	# 4 NC	12 NC	# 4 NYDQ4	12*NYDQ7
# 5 SDQ1	13 YDQ3	# 5 XCLK/2	13 NC	# 5*NYDQ5	13 YDQ7
# 6 YDQ1	14 SDQ3	# 6*YCLK/2	14 VCC	# 6 YDQ5	14 NYDQ7
# 7 SDQ1	15 YSDIEN	# 7 GND		# 7 NYDQ5	15 YDIEN
# 8 GND	16 VCC	# 8 NC		# 8 GND	16 VCC

```
#################################################################################
#D:16                          #D:18                          #D:21            #
#7400 NAND3                    #74C42 DCT32                   #7427 3-NOR      #
# 1 /XA131415    9 /YRDSEL     # 1 XA131415     9 YMREQ       # 1 XA15     9 YA13  #
# 2 /XMREQ      10 YWRSEL      # 2*NXA131415   10*NYRDSEL     # 2 XA14    10 YA14  #
# 3*XARBIT      11*XSDIEN      # 3 YA131415    11 YRDSEL      # 3 NC      11 YA15  #
# 4 /YMREQ      12 XWRSEL      # 4*NYA131415   12*NXRDSEL     # 4 NC      12*XA131415 #
# 5 /YA131415   13 /XRDSEL     # 5 XMREQ       13 XRDSEL      # 5 NC      13 XA13  #
# 6*YARBIT      14 VCC         # 6*NXMREQ      14 VCC         # 6 NC      14 VCC   #
# 7 GND                        # 7 GND                        # 7 GND            #
# 8*YSDIEN                     # 8*NYMREQ                     # 8*YA131415       #
#################################################################################
#E:23                          #E:11                          #E:12            #
#7413--36                      #7432 2-OR                     #7432 2-OR       #
# 1 A13          9*CE-SC000    # 1 XSEL         9 YWR         # 1 CE-XY2000  9 CE-XY6000 #
# 2 A14         10*CE-SA000    # 2 XWR         10 YSEL        # 2 YSEL      10 YSEL  #
# 3 A15         11*CE-SE0CC    # 3*XWRSEL      11*YRDSEL      # 3*CS-Y2000  11 NC    #
# 4 GND         12*CE-XY6000   # 4 XSEL        12 YSEL        # 4 CE-XY4000 12 NC    #
# 5 GND         13*CE-XY4000   # 5 XRD         13 YRD         # 5 YSEL      13 NC    #
# 6 VCC         14*CE-XY2000   # 6*XRDSEL      14 VCC         # 6*CS-Y4000  14 VCC   #
# 7*CE-SE000    15 NC          # 7 GND                        # 7 GND            #
# 8 GND         16 VCC         # 8*YWRSEL                     # 8*CS-Y6000       #
#################################################################################
#E:13                          #E:15                          #E:17            #
#74126 YDATA                   #74126-41                      #7400NAND43      #
# 1 CS-YDATA     9* YDQ2       # 1 YSEL         9 NC          # 1 NXSEL    9 NC  #
# 2*YDQ0        10 YDQ2        # 2 XARBIT      10 NC          # 2 CE-XY    10 NC #
# 3 YDQ0        11 /YDQ2       # 3*XSEL        11 NC          # 3*CS-XDATA 11 NC #
# 4 /YDQ0       12* YDQ3       # 4 XSEL        12 NC          # 4 CE-XY    12 NC #
# 5*/YDQ1       13 YDQ3        # 5 YARBIT      13 NC          # 5 NYSEL    13 NC #
# 6 YDQ1        14 /YDQ3       # 6*YSEL        14 VCC         # 6*CS-YDATA 14 VCC #
# 7 /YDQ1       15 YDIEN       # 7 GND                        # 7 GND            #
# 8 GND         16 VCC         # 8 NC                         # 8 NC             #
#################################################################################
```

#F:15
#74367-53

# 1 GND	9*NYA3	# 1 GND	9 NC
# 2 YA7	10 YA3	# 2 XA12	10 NC
# 3*NYA6	11*NYA4	# 3*NXA12	11 NC
# 4 YA1	12 YA4	# 4 YA12	12 NC
# 5*NYA1	13*NYA5	# 5*NYA12	13 NC
# 6 YA2	14 YA5	# 6 NC	14 NC
# 7*NYA2	15 GND	# 7 NC	15 GND
# 8 GND	16 VCC	# 8 GND	16 VCC

#F:16
#74367-54

# 1 GND	9 NC	# 1 VCC	9 Y15
# 2 XA12	10 NC	# 2 NYOE	10 NYSEL
# 3*NXA12	11 NC	# 3 NC	11 VCC
# 4 YA12	12 NC	# 4 NC	12*YDIEN
# 5*NYA12	13 NC	# 5 NC	13 YWE
# 6 NC	14 NC	# 6 NC	14 VCC
# 7 NC	15 GND	# 7 GND	
# 8 GND	16 VCC	# 8*CS-SYDATA	

#F:17
#7408-2AND

# 1 XSEL	9 YRDSEL	# 1 XSEL	9 YRDSEL
# 2 YSEL	10 XRDSEL	# 2 YSEL	10 XRDSEL
# 3*STROBE	11 NC	# 3*STROBE	11 NC
# 4 XWRSEL	12 NC	# 4 XWRSEL	12 NC
# 5 YWRSEL	13 NC	# 5 YWRSEL	13 NC
# 6*WR-SHARE	14 VCC	# 6*WR-SHARE	14 VCC
# 7 GND		# 7 GND	
# 8*RD-SHARE		# 8*RD-SHARE	

#F:18
#7408-2AND

# 1 XSEL	9 YWRSEL	# 1 XSEL	9 YWRSEL
# 2 YSEL	10 XWRSEL	# 2 YSEL	10 XWRSEL
# 3*STROBE	11 NC	# 3*STROBE	11 NC
# 4 XRDSEL	12 NC	# 4 XRDSEL	12 NC
# 5 YRDSEL	13 NC	# 5 YRDSEL	13 NC
# 6*WR-SHARE	14 VCC	# 6*WR-SHARE	14 VCC
# 7 GND		# 7 GND	
# 8*RD-SHARE		# 8*RD-SHARE	

#F:19
#7408-2AND

# 1 XSEL	9 YSEL	# 1 XSEL	9 YSEL
# 2 YSEL	10 XSEL	# 2 YSEL	10 XSEL
# 3*STROBE	11 NC	# 3*STROBE	11 NC
# 4 XWRSEL	12 NC	# 4 XWRSEL	12 NC
# 5 YWRSEL	13 NC	# 5 YWRSEL	13 NC
# 6*WR-SHARE	14 VCC	# 6*WR-SHARE	14 VCC
# 7 GND		# 7 GND	
# 8*RD-SHARE		# 8*RD-SHARE	

#F:20
#7408-2AND

# 1 XSEL	9 YSEL	# 1 XSEL	9 YSEL
# 2 YSEL	10 XSEL	# 2 YSEL	10 XSEL
# 3*STROBE	11 NC	# 3*STROBE	11 NC
# 4 XRDSEL	12 NC	# 4 XRDSEL	12 NC
# 5 YRDSEL	13 NC	# 5 YRDSEL	13 NC
# 6*WR-SHARE	14 VCC	# 6*WR-SHARE	14 VCC
# 7 GND		# 7 GND	
# 8*RD-SHARE		# 8*RD-SHARE	

#F:18
#74367-56

# 1 GND	9*NXA9	#
# 2 XA6	10 XA8	#
# 3*NXA6	11*NXA10	#
# 4 XA7	12 XA10	#
# 5*NXA7	13*NXA11	#
# 6 XA5	14 XA11	#
# 7*NXA5	15 GND	#
# GND	16 VCC	#

#F:19
#74367-57

# 1 GND	9*NXA3	#
# 2 XA0	10 XA3	#
# 3*NXA0	11*NXA4	#
# 4 XA1	12 XA4	#
# 5*NXA1	13*NXA5	#
# 6 XA2	14 XA5	#
# 7*NXA2	15 GND	#
# GND	16 VCC	#

#F:21
#74367-59

# 1 GND	9*XOE	#
# 2 YW9	10 XRD	#
# 3*YWF	11*X15	#
# 4 XW9	12 XA15	#
# 5*XWE	13*Y15	#
# 6 YRD	14 YA15	#
# 7*YOE	15 GND	#
# 8 GND	16 VCC	#

#F:22
#7410-3NAND

# 1 VCC	9 Y15	#
# 2 NXSEL	10 NXSEL	#
# 3 CS-XY4000	11 VCC	#
# 4 CS-XY4800	12*XDIEN	#
# 5 CS-XY2800	13 XWE	#
# 6*CS-XY	14 VCC	#
# 7 GND		#
# 8*CS-NXDATA		#

#F:23
#8216 XDATA

# 1 CS-XDATA	9*NXDQ2	#
# 2*NXDQ0	10 XDQ2	#
# 3 XDQ0	11 NXDQ2	#
# 4 NXDQ0	12*NXDQ3	#
# 5*NXDQ1	13 XDQ3	#
# 6 XDQ1	14 NXDQ3	#
# 7 NXDQ1	15 XDIEN	#
# 8 GND	16 VCC	#

#G:1
#Y-2[illegible]

# 1 NC	9 NXA1	17 NXDQ5	25 NXA8
# 2 NXA12	10 NXA0	18 NXDQ6	26 NC
# 3 NXA7	11 NXDQ0	19 NXDQ7	27 XWE
# 4 NXA6	12 NXDQ1	20 CS-X2000	28 VCC
# 5 NXA5	13 NXDQ2	21 NXA10	
# 6 NXA4	14 GND	22 XOE	
# 7 NXA3	15 NXDQ3	23 NXA11	
# NXA2	16 NXDQ4	24 NXA9	

```
##########################################################################################
# :.                                                                                     #
#.-4(                                                                                    #
# 1 NC               9 NXA1         17 NXDQ5        25 NXA8                              #
# 2 NXA12           10 NXA0         18 NXDQ6        26 NC                                #
# 3 NXA7            11 NXDQ0        19 NXDQ7        27 XWE                               #
# 4 NXA6            12 NXDQ1        20 CS-X4000     28 VCC                               #
# 5 NXA5            13 NXDQ2        21 NXA10                                             #
# 6 NXA4            14 GND          22 XOE                                               #
# 7 NXA3            15 NXDQ3        23 NXA11                                             #
# 8 NXA2            16 NXDQ4        24 NXA9                                              #
##########################################################################################
#G:3                                                                                     #
#X-6000                                                                                  #
# 1 NC               9 NXA1         17 NXDQ5        25 NXA8                              #
# 2 NXA12           10 NXA0         18 NXDQ6        26 NC                                #
# 3 NXA7            11 NXDQ0        19 NXDQ7        27 XWE                               #
# 4 NXA6            12 NXDQ1        20 CS-X6000     28 VCC                               #
# 5 NXA5            13 NXDQ2        21 NXA10                                             #
# 6 NXA4            14 GND          22 XCE                                               #
# 7 NXA3            15 NXDQ3        23 NXA11                                             #
# 8 NXA2            16 NXDQ4        24 NXA9                                              #
##########################################################################################
#H:1                                                                                     #
#Y-2000                                                                                  #
# 1 NC               9 NYA1         17 NYDQ5        25 NYA8                              #
# 2 NYA12           10 NYA0         18 NYDQ6        26 NC                                #
# 3 NYA7            11 NYDQ0        19 NYDQ7        27 YWE                               #
# 4 NYA6            12 NYDQ1        20 CS-Y2000     28 VCC                               #
# 5 NYA5            13 NYDQ2        21 NYA10                                             #
# 6 NYA4            14 GND          22 YCE                                               #
# 7 NYA3            15 NYDQ3        23 NYA11                                             #
# 8 NYA2            16 NYDQ4        24 NYA9                                              #
##########################################################################################
```

```
##################################################################################
#H:2                                                                             #
#Y-400?                                                                          #
# 1 N.C          9 NYA1        17 NYDQ5       25 NYA8                           #
# 2 NYA12       10 NYAC        18 NYDQ6       26 N.C                            #
# 3 NYA7        11 NYDQ0       19 NYDQ7       27 YWE                            #
# 4 NYA6        12 NYDQ1       20 CS-Y4000    28 VCC                            #
# 5 NYA5        13 NYDQ2       21 NYA10                                         #
# 6 NYA4        14 GND         22 YOE                                           #
# 7 NYA3        15 NYDQ3       23 NYA11                                         #
#   NYA2        16 NYDQ4       24 NYA9                                          #
##################################################################################
#H:3                                                                             #
#Y-6000                                                                          #
# 1 N.C          9 NYA1        17 NYDQ5       25 NYA8                           #
# 2 NYA12       10 NYAC        18 NYDQ6       26 NC                             #
# 3 NYA7        11 NYDQ0       19 NYDQ7       27 YWE                            #
# 4 NYA6        12 NYDQ1       20 CS-Y6000    28 VCC                            #
# 5 NYA5        13 NYDQ2       21 NYA10                                         #
# 6 NYA4        14 GND         22 YOE                                           #
# 7 NYA3        15 NYDQ3       23 NYA11                                         #
#   NYA2        16 NYDQ4       24 NYA9                                          #
##################################################################################
#H:4                                                                             #
#S-5???                                                                          #
# 1 NC           9 A1          17 SDQ5        25 A8                             #
# 2 A12         10 A?          18 SDQ6        26 NC                             #
# 3 A7          11 SDQ0        19 SDQ7        27 WR-SHARE                       #
# 4 A6          12 SDQ1        20 CS-S8000    28 VCC                            #
# 5 A5          13 SDQ2        21 A10                                           #
# 6 A4          14 GND         22 RD-SHARE                                      #
# 7 A3          15 SDQ3        23 A11                                           #
#   A2          16 SDQ4        24 A9                                            #
##################################################################################
```

```
#H:5
#S-ACC1
# 1 NC          9 A1          17 SDQ5       25 A8
# 2 A12        10 A0          18 SDQ6       26 NC
# 3 A7         11 SDQ0        19 SDQ7       27 WR-SHARE
# 4 A6         12 SDQ1        20 CE-SA000   28 VCC
# 5 A5         13 SDQ2        21 A10
# 6 A4         14 GND         22 RD-SHARE
# 7 A3         15 SDQ3        23 A11
# 8 A2         16 SDQ4        24 A9
#H:6
#S-CC01
# 1 NC          9 A1          17 SDQ5       25 A8
# 2 A12        10 A0          18 SDQ6       26 NC
# 3 A7         11 SDQ0        19 SDQ7       27 WR-SHARE
# 4 A6         12 SDQ1        20 CE-SC000   28 VCC
# 5 A5         13 SDQ2        21 A10
# 6 A4         14 GND         22 RD-SHARE
# 7 A3         15 SDQ3        23 A11
# 8 A2         16 SDQ4        24 A9
#H:7
#S-EC01
# 1 NC          9 A1          17 SDQ5       25 A8
# 2 A12        10 A0          18 SDQ6       26 NC
# 3 A7         11 SDQ0        19 SDQ7       27 WR-SHARE
# 4 A6         12 SDQ1        20 CE-SE000   28 VCC
# 5 A5         13 SDQ2        21 A10
# 6 A4         14 GND         22 RD-SHARE
# 7 A3         15 SDQ3        23 A11
# 8 A2         16 SDQ4        24 A9
```

SIGNAL LIST FOR UNID MEMORY CARD PAGE 1

SIGNAL	FANOUT	SOURCE	SINKS			
A0	4	B:16/12	H:4/10	H:5/10	H:6/10	H:7/10
A1	4	B:16/9	H:4/9	H:5/9	H:6/9	H:7/9
A10	4	B:21/7	H:4/21	H:5/21	H:6/21	H:7/21
A11	4	B:21/4	H:4/23	H:5/23	H:6/23	H:7/23
A12	4	B:23/12	H:4/2	H:5/2	H:6/2	H:7/2
A13	1	B:23/9	D:23/1			
A14	1	B:23/7	D:23/2			
A15	1	B:23/4	D:23/3			
A2	4	B:16/7	H:4/8	H:5/8	H:6/8	H:7/8
A3	4	B:16/4	H:4/7	H:5/7	H:6/7	H:7/7
A4	4	B:16/12	H:4/6	H:5/6	H:6/6	H:7/6
A5	4	B:16/9	H:4/5	H:5/5	H:6/5	H:7/5
A6	4	B:16/7	H:4/4	H:5/4	H:6/4	H:7/4
A7	4	B:16/4	H:4/3	H:5/3	H:6/3	H:7/3

SIGNAL	FANOUT	SOURCE	SINKS			
A8	4	B:21/12	H:4/25	H:5/25	H:6/25	H:7/25
A9	4	B:21/9	H:4/24	H:5/24	H:6/24	H:7/24
CE-S8000	1	D:23/11	H:4/20			
CE-SA000	1	D:23/10	H:5/20			
CE-SC000	1	D:23/9	H:6/20			
CE-SE000	1	D:23/7	H:7/20			
CE-XY	2	F:22/6	E:17/2,4			
CE-XY2000	3	D:23/14	E:12/1	F:12/1	F:22/5	
CE-XY4000	3	D:23/13	E:12/4	F:12/4	F:22/4	
CE-XY6000	3	D:23/12	E:12/9	F:12/9	F:22/3	
CS-SXDATA	2	F:22/8	B:11/1	C:12/1		
CS-SYDATA	2	F:11/8	B:13/1	C:14/1		
CS-X2000	1	F:12/3	G:1/20			
CS-X4000	1	F:12/6	G:2/20			
CS-X6000	1	F:12/8	G:3/20			

SIGNAL	FANOUT	SOURCE	SINKS
CS-XDATA	2	E:17/3	E:23/1 F:23/1
CS-Y2000	1	E:12/3	H:1/20
CS-Y4000	1	E:12/6	H:2/20
CS-Y6000	1	E:12/8	H:3/20
CS-YDATA	2	E:17/6	D:13/1 E:13/1
GND	57	A:1/120	B:11/8 B:13/8 B:16/8 B:18/8 B:21/8 B:23/8 C:12/8 C:14/8 C:17/7 D:13/8 D:16/7 D:18/7 D:21/7 D:23/4,5,8 E:11/7 E:12/7 E:13/8 E:15/7 E:17/7 E:19/7 E:23/8 F:11/7 F:12/7 F:13/7 F:14/1,8,15 F:15/1 F:15/8,15 F:16/1,8,15 F:17/7 F:18/1,8,15 F:19/1,8,15 F:21/1,8,15 F:22/7 F:23/8 G:1/14 G:2/14 G:3/14 H:1/14 H:2/14 H:3/14 H:4/14 H:5/14 H:6/14 H:7/14
LXA0	3	F:1[illegible]/3	G:1/10 G:2/10 G:3/10
LXA1	3	F:1[illegible]/5	G:1/9 G:2/9 G:3/9
LXA10	3	F:1[illegible]/11	G:1/21 G:2/21 G:3/21
LXA11	3	F:1[illegible]/13	G:1/23 G:2/23 G:3/23
LXA12	3	F:16/3	G:1/2 G:2/2 G:3/2
LXA13I+15	1	D:1[illegible]/2	D:16/1
LXA2	3	F:1[illegible]/7	G:1/[illegible] G:2/[illegible] G:3/[illegible]

SIGNAL	FANOUT	SOURCE	SINKS
MXA3	3	F:1?/?	G:1/7 G:2/7 G:3/7
MXA4	3	F:1 /11	G:1/6 G:2/6 G:3/6
MXA5	3	F:1 /13	G:1/5 G:2/5 G:3/5
MXA6	3	F:1 /3	G:1/4 G:2/4 G:3/4
MXA7	3	F:1 /5	G:1/3 G:2/3 G:3/3
MXA8	3	F:1 /7	G:1/25 G:2/25 G:3/25
MXA9	3	F:1 /9	G:1/24 G:2/24 G:3/24
MXDQ0	4	F:23/2	F:23/4 G:1/11 G:2/11 G:3/11
MXDQ1	4	F:23/5	F:23/7 G:1/12 G:2/12 G:3/12
MXDQ2	4	F:23/9	F:23/11 G:1/13 G:2/13 G:3/13
MXDQ3	4	F:23/12	F:23/14 G:1/15 G:2/15 G:3/15
MXDQ4	4	E:23/2	E:23/4 G:1/16 G:2/16 G:3/16
MXDQ5	4	E:23/5	E:23/7 G:1/17 G:2/17 G:3/17
MXDQ6	4	E:23/9	E:23/11 G:1/18 G:2/18 G:3/18
MXDQ7	4	E:23/12	E:23/14 G:1/19 G:2/19

SIGNAL	FANOUT	SOURCE	SINKS G:3/19
NXMREQ	1	D:1 /6	D:16/2
NXME	1	E:1 /2	F:22/2
NXMDSEL	1	D:1 /12	D:16/13
NXSEL	2	E:1 /6	E:17/1 F:22/10
NYA0	3	F:15/3	H:1/10 H:2/10 H:3/10
NYA1	3	F:15/5	H:1/9 H:2/9 H:3/9
NYA10	3	F:14/11	H:1/21 H:2/21 H:3/21
NYA11	3	F:14/13	H:1/23 H:2/23 H:3/23
NYA12	3	F:16/5	H:1/2 H:2/2 H:3/2
NYA13141S	1	D:1 /4	D:16/5
NYA2	3	F:15/7	H:1/8 H:2/8 H:3/8
NYA3	3	F:15/9	H:1/7 H:2/7 H:3/7
NYA4	3	F:15/11	H:1/6 H:2/6 H:3/6
NYA5	3	F:15/13	H:1/5 H:2/5 H:3/5
NYA6	3	F:14/3	H:1/4 H:2/4 H:3/4
NYA7	3	F:14/5	H:1/3 H:2/3 H:3/3

SIGNAL	FANOUT	SOURCE	SINKS			
MYA8	3	F:14/7	H:1/25	H:2/25	H:3/25	
MYA9	3	F:14/9	H:1/24	H:2/24	H:3/24	
MYDQ0	4	E:13/2	E:13/4	H:1/11	H:2/11	H:3/11
MYDQ1	4	E:13/5	E:13/7	H:1/12	H:2/12	H:3/12
MYDQ2	4	E:13/9	E:13/11 H:3/13	H:1/13	H:2/13	
MYDQ3	4	E:13/12	E:13/14 H:3/15	H:1/15	H:2/15	
MYDQ4	4	D:13/2	D:13/4	H:1/16	H:2/16	H:3/16
MYDQ5	4	D:13/5	D:13/7	H:1/17	H:2/17	H:3/17
MYDQ6	4	D:13/9	D:13/11 H:3/18	H:1/18	H:2/18	
MYDQ7	4	D:13/12	D:13/14 H:3/19	H:1/19	H:2/19	
MYPEN	1	D:15/5	D:16/4			
MYWE	1	E:15/6	F:11/2			
MY_DSEL	1	D:15/10	D:16/9			
MY_EL	2	E:15/12	E:17/5	F:11/10		

SIGNAL	FANOUT	SOURCE	SINKS
RD-SHARE	4	F:17/3	H:4/22 H:5/22 H:6/22 H:7/22
SDD0	7	C:12/2	C:12/4 C:14/2,4 H:4/11 H:5/11 H:6/11 H:7/11
SDD1	7	C:12/5	C:12/7 C:14/5,7 H:4/12 H:5/12 H:6/12 H:7/12
SDD2	7	C:12/9	C:12/11 C:14/9,11 H:4/13 H:5/13 H:6/13 H:7/13
SDD3	7	C:12/12	C:12/14 C:14/12,14 H:4/15 H:5/15 H:6/15 H:7/15
SDD4	7	B:11/2	B:11/4 B:13/2,4 H:4/16 H:5/16 H:6/16 H:7/16
SDD5	7	B:11/5	B:11/7 B:13/5,7 H:4/17 H:5/17 H:6/17 H:7/17
SDD6	7	B:11/9	B:11/11 B:13/9,11 H:4/18 H:5/18 H:6/18 H:7/18
SDD7	7	B:11/12	B:11/14 B:13/12,14 H:4/19 H:5/19 H:6/19 H:7/19
SYSRST	4	F:17/3	B:16/15 B:17/15 B:21/15 B:23/15
VCC	48	A:1/60	B:11/16 B:13/16 B:16/14 B:17/16 B:21/16 B:23/14 C:12/16 C:14/16 C:17/14 D:13/16 D:16/14 D:18/14 D:21/14 D:23/6,16 E:11/14 E:12/14 E:13/16 E:15/14 E:17/14 E:19/14 E:23/16 F:11/1,11,14 F:12/14 F:13/14 F:14/16 F:15/16 F:16/14 F:17/14 F:18/16 F:19/16

SIGNAL LIST FOR UNIT MEMORY CARD PAGE 8

SIGNAL	FANOUT	SOURCE	SINKS			
			F:21/16	F:22/1,11,14		F:23/16
			G:1/28	G:2/28	G:3/28	H:1/28
			H:2/28	H:3/28	H:4/28	H:5/28
			H:6/28	H:7/28		
WR-SHAPE	4	F:1/6	H:4/27	H:5/27	H:6/27	H:7/27
X1[illegible]	1	F:21/11	F:22/9			
XA	2	A:1/90	B:16/13	F:19/2		
XA1	2	A:1/92	B:16/10	F:19/4		
XA10	2	A:1/33	B:21/6	F:18/12		
XA11	2	A:1/35	B:21/3	F:18/14		
XA12	2	A:1/30	B:23/13	F:16/2		
XA13	2	A:1/32	B:23/10	D:21/13		
XA13141[illegible]	1	D:21/12	D:16/1			
XA14	2	A:1/34	B:23/6	D:21/2		
XA15	3	A:1/36	B:23/3	D:21/1	F:21/12	
XA	2	A:1/94	B:16/6	F:19/6		
XA[illegible]	2	A:1/[illegible]8	B:16/3	F:19/10		
XA4	2	A:1/91	B:16/13	F:19/12		

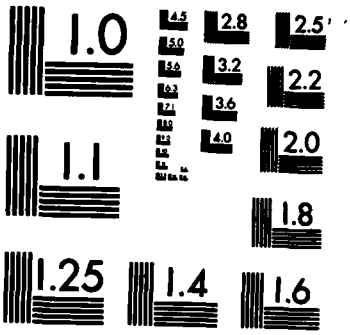
SIGNAL	FANOUT	SOURCE	SINKS
XA	2	A:1/93	B:18/10 F:19/14
XA	2	A:1/95	B:18/6 F:18/2
XA7	2	A:1/97	B:18/3 F:16/4
XA	2	A:1/29	B:21/13 F:15/6
XA	2	A:1/31	B:21/10 F:18/10
XA BIT	2	D:16/3	E:15/2 F:13/9
XCLK/2	1	A:1/56	C:17/5
XDIR	2	F:23/12	E:23/15 F:23/15
XD00	2	A:1/	C:12/3 F:23/3
XD01	2	A:1/6	C:12/6 F:23/6
XD02	2	A:1/7	C:12/10 F:23/10
XD03	2	A:1/	C:12/13 F:23/13
XD04	2	A:1/70	B:11/3 E:23/3
XD05	2	A:1/71	B:11/6 F:23/6
XD06	2	A:1/	B:11/10 F:23/10
XD07	2	A:1/1	B:11/13 F:23/13
XDLG	1	A:1/11	D:1 /5

SIGNAL	FANOUT	SOURCE	SINKS
XLE	4	F:21/[illegible]	E:19/1 G:1/22 G:2/22 G:3/22
XMD	2	A:1/111	E:11/5 F:21/10
XMDSEL	2	E:11/6	D:16/13 F:17/10
XMDSEL	2	D:16/11	B:11/15 C:12/15
XSEL	9	E:15/3	E:11/1,4 E:15/4 E:13/5 F:12/2,5,10 F:15/2 F:17/1
XWAIT	1	F:13/6	A:1/55
XW[illegible]	4	F:21/5	F:22/13 G:1/27 G:2/27 G:3/27
XW	2	A:1/117	F:11/2 F:21/4
XW[illegible]SEL	2	E:11/3	D:16/12 F:17/4
XYA[illegible]	2	F:13/[illegible]	F:13/1,[illegible]
Y1	1	F:21/15	F:11/9
YA	2	A:1/[illegible]	B:16/14 F:15/2
YA[illegible]	2	A:1/102	B:16/11 F:15/4
Y[illegible]	2	A:1/43	B:21/5 F:14/12
YA[illegible]1	2	A:1/45	B:21/2 F:14/14
YA[illegible]	2	A:1/4[illegible]	B:23/14 F:15/4

SIGNAL	FANOUT	SOURCE	SINKS
YA13	2	A:1/42	B:23/11 D:21/9
YA131415	1	D:21/8	D:19/3
YA14	2	A:1/44	B:23/5 D:21/10
YA15	3	A:1/46	B:23/2 D:21/11 F:21/14
YA2	2	A:1/104	B:16/5 F:15/6
YA3	2	A:1/106	B:16/2 F:15/10
YA4	2	A:1/101	B:16/14 F:15/12
YA5	2	A:1/103	B:16/11 F:15/14
YA6	2	A:1/105	B:16/5 F:14/2
YA7	2	A:1/107	B:16/2 F:14/4
YA8	2	A:1/34	B:21/14 F:14/6
YA9	2	A:1/41	B:21/11 F:14/10
YA BIT	2	D:16/6	E:19/5 F:13/10
YCLK/2	1	C:1//5	A:1/56
YD BIT	2	F:11/13	D:13/15 F:13/16
YDMA	2	A:1/74	C:14/3 F:13/3
YDMA1	2	A:1/73	C:14/4 F:13/4

AD-A126 031 CONTINUED DEVELOPMENT OF THE UNIVERSAL NETWORK INTERFACE DEVICE(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGINEERING G CUOMO 2/2

UNCLASSIFIED DEC 82 AFIT/GE/EE/82D-28 F/G 9/2 NL



SIGNAL	FANOUT	SOURCE	SINKS
YD02	2	A:1/13	C:14/10 E:13/10
YD03	2	A:1/14	C:14/13 E:13/13
YD04	2	A:1/76	B:13/3 D:13/3
YD05	2	A:1/77	B:13/6 D:13/6
YD06	2	A:1/15	B:13/10 D:13/10
YD07	2	A:1/16	B:13/13 D:13/13
YM-EQ	1	A:1/112	D:15/9
YOF	4	F:21/7	E:19/9 H:1/22 H:2/22 H:3/22
YRD	2	A:1/113	E:11/13 F:21/6
YRDSEL	2	E:11/11	D:18/11 F:17/9
YRDIEL	2	D:16/8	B:13/15 C:14/15
YSEL	13	E:15/6	B:16/1 B:17/1 B:21/1 B:23/1 E:11/10,12 E:12/2,5,10 E:15/1 E:19/13 F:13/4 F:17/2
YWAIT	1	F:13/3	A:1/57
YWF	4	F:21/3	F:11/13 H:1/27 H:2/27 H:3/27
YW-	2	A:1/115	E:11/9 F:21/2

SIGNAL LIST FOR UNIX MEMORY CARD PAGE 13

SIGNAL	FANOUT	SOURCE	SINKS
YW-SEL	2	E:11/8	D:16/10 F:17/5

A:1/36	B:23/3	XA15
A:1/46	B:23/2	YA15
A:1/55	F:13/6	XWAIT
A:1/56	C:17/5	XCLK/2
A:1/57	F:13/3	YWAIT
A:1/58	C:17/6	YCLK/2
A:1/110	D:16/5	XMREQ
A:1/112	D:16/3	YMREQ
B:11/1	C:12/1	CS-SXDATA
B:11/2	B:11/4	SDQ4
B:11/3	E:23/3	XDQ4
B:11/5	B:11/7	SDQ5
B:11/6	E:23/6	XDQ5
B:11/9	B:11/11	SDQ6
B:11/10	E:23/10	XDQ6
B:11/12	B:11/14	SDQ7
B:11/13	E:23/13	XDQ7
B:11/15	C:12/15	XSDIEN
B:13/1	C:14/1	CS-SYDATA
B:13/2	B:13/4	SDQ4
B:13/3	D:13/3	YDQ4
B:13/5	B:13/7	SDQ5
B:13/6	D:13/6	YDQ5
B:13/9	B:13/11	SDQ6
B:13/10	D:13/10	YDQ6
B:13/12	B:13/14	SDQ7
B:13/13	D:13/13	YDQ7
B:13/15	C:14/15	YSDIEN
B:16/1	B:13/1	YSFL
B:16/2	F:15/10	YA3
B:16/3	F:19/10	XA3
B:16/5	F:15/5	YA2
B:16/6	F:19/6	XA2
B:16/10	F:19/4	XA1
B:16/11	F:15/4	YA1
B:16/13	F:19/2	XA0
B:16/14	F:15/2	YA0
B:16/15	B:15/15	STROBE
B:16/2	F:14/4	YA7

B:16/3	F:16/4	XA7
B:18/5	F:14/2	YA6
B:18/6	F:18/2	XA6
B:18/10	F:19/14	XA5
B:18/11	F:15/14	YA5
B:18/13	F:19/12	XA4
B:18/14	F:15/12	YA4

B:21/1	B:23/1	YSEL
B:21/2	F:14/14	YA11
B:21/3	F:16/14	XA11
B:21/5	F:14/12	YA10
B:21/6	F:18/12	XA10
B:21/10	F:18/10	XA9
B:21/11	F:14/10	YA9
B:21/13	F:16/6	XA8
B:21/14	F:14/6	YA8
B:21/15	B:23/15	STROBE

B:23/4	D:23/3	A15
B:23/5	D:21/16	YA14
B:23/6	D:21/2	XA14
B:23/7	D:23/2	A14
B:23/9	D:23/1	A13
B:23/10	D:21/15	XA13
B:23/11	D:21/9	YA13
B:23/13	F:16/2	XA12
B:23/14	F:16/4	YA12

C:12/2	C:12/4	SDQ0
C:12/3	F:23/3	XDQ0
C:12/5	C:12/7	SDQ1
C:12/6	F:23/6	XDQ1
C:12/9	C:12/11	SDQ2
C:12/10	F:23/10	XDQ2
C:12/12	C:12/14	SDQ3
C:12/13	F:23/13	XDQ3

C:14/2	C:14/4	SDQ0
C:14/3	C:13/3	YDQ0
C:14/5	C:14/7	SDQ1
C:14/6	C:13/6	YDQ1
C:14/9	C:14/11	SDQ2
C:14/10	C:13/10	YDQ2

C:14/12	C:14/14	SDQ3
C:14/13	E:13/13	YDQ3
D:13/1	E:13/1	CS-YDATA
D:13/4	H:1/16	NYDQ4
D:13/7	H:1/17	NYDQ5
D:13/11	H:1/19	NYDQ6
D:13/14	H:1/13	NYDQ7
D:13/15	E:13/15	YDIEN
D:16/1	D:18/2	NXA131415
D:16/2	D:18/6	NXMREQ
D:16/4	D:18/8	NYMREQ
D:16/5	D:18/4	NYA131415
D:16/9	D:18/10	NYRDSEL
D:16/10	F:17/5	YWRSEL
D:16/12	F:17/4	XWRSEL
D:16/13	D:18/12	NXRDSEL
D:18/1	D:21/12	XA131415
D:18/5	D:21/8	YA131415
D:16/11	F:17/9	YRDSEL
D:18/15	F:17/10	XRDSEL
D:21/1	F:21/12	XA15
D:21/11	F:21/14	YA15
D:23/7	H:7/20	CE-SE000
D:23/9	H:6/20	CE-SC000
D:23/10	H:5/20	CE-SA000
D:23/12	H:4/20	CE-S8000
D:23/12	F:22/3	CE-XY6000
D:23/13	F:22/4	CE-XY4000
D:23/14	F:22/5	CE-XY2000
E:11/1	E:11/4	XSEL
E:11/2	F:21/4	XWR
E:11/5	F:21/10	XRD
F:11/9	F:21/2	YWR
E:11/12	E:12/10	YSEL
F:11/12	F:13/4	YSEL
E:11/13	F:21/6	YRD

E:12/1	F:12/1	CE-XY2000
E:12/2	E:12/5	YSEL
E:12/3	H:1/20	CS-Y2000
E:12/4	F:12/4	CE-XY4000
E:12/6	H:2/20	CS-Y4000
E:12/8	H:3/20	CS-Y6000
E:12/9	F:12/9	CE-XY6000
E:13/4	H:1/11	NYDQ0
F:13/7	H:1/12	NYDQ1
E:13/11	H:1/13	NYDQ2
E:13/14	H:1/15	NYDQ3
E:15/1	E:15/6	YSEL
E:15/2	F:13/9	XARBIT
E:15/3	E:15/4	XSEL
E:15/5	F:13/10	YARBIT
E:17/1	E:19/6	NXSEL
E:17/2	E:17/4	CE-XY
E:17/5	F:11/10	NYSEL
E:19/1	F:21/9	XCE
E:19/2	F:22/2	NXOE
F:19/5	F:17/1	XSEL
F:19/8	F:11/2	NYOE
E:19/9	F:21/1	YCE
E:19/13	F:17/2	YSEL
E:23/1	F:23/1	CS-XDATA
E:23/4	G:1/16	NXDQ4
E:23/7	G:1/17	NXDQ5
E:23/11	G:1/18	NXDQ6
E:23/14	G:1/19	NXDQ7
E:23/15	F:23/15	XDIEN
F:11/4	F:21/13	Y15
F:11/12	F:21/5	YWE
F:12/2	F:13/2	XSEL

F:12/3	G:1/26	CS-X2000
F:12/5	E:15/3	XSEL
F:12/6	G:2/20	CS-X4000
F:12/4	G:3/20	CS-X6000
F:13/1	F:13/5	XYARHIT
F:14/3	H:1/4	NYA6
F:14/5	H:1/3	NYA7
F:14/7	H:1/28	NYA8
F:14/9	H:1/24	NYA9
F:14/11	H:1/21	NYA10
F:14/13	H:1/23	NYA11
F:15/3	H:1/10	NYA0
F:15/5	H:1/9	NYA1
F:15/7	H:1/8	NYA2
F:15/9	H:1/7	NYA3
F:15/11	H:1/6	NYA4
F:15/13	H:1/5	NYA5
F:16/3	G:1/2	NXA12
F:16/5	H:1/2	NYA12
F:18/3	G:1/4	NXA6
F:18/5	G:1/3	NXA7
F:18/7	G:1/28	NXA8
F:18/9	G:1/24	NXA9
F:18/11	G:1/21	NXA10
F:18/13	G:1/23	NXA11
F:19/3	G:1/10	NXA0
F:19/5	G:1/9	NXA1
F:19/7	G:1/8	NXA2
F:19/9	G:1/7	NXA3
F:19/11	G:1/6	NXA4
F:19/13	G:1/5	NXA5
F:21/11	F:22/9	X15
F:22/13	G:1/27	XWE

F:23/4	G:1/11	NXDQ0
F:23/7	G:1/12	NXDQ1
F:23/11	G:1/13	NXDQ2
F:23/14	G:1/15	NXDQ3
G:1/22	G:2/22	XOE
G:2/2	G:3/2	NXA12
G:2/3	G:3/3	NXA7
G:2/4	G:3/4	NXA6
G:2/5	G:3/5	NXA5
G:2/6	G:3/6	NXA4
G:2/7	G:3/7	NXA3
G:2/8	G:3/8	NXA2
G:2/9	G:3/9	NXA1
G:2/10	G:3/10	NXA0
G:2/11	G:3/11	NXDQ0
G:2/12	G:3/12	NXDQ1
G:2/13	G:3/13	NXDQ2
G:2/15	G:3/15	NXDQ3
G:2/16	G:3/16	NXDQ4
G:2/17	G:3/17	NXDQ5
G:2/18	G:3/18	NXDQ6
G:2/19	G:3/19	NXDQ7
G:2/21	G:3/21	NXA10
G:2/23	G:3/23	NXA11
G:2/24	G:3/24	NXA9
G:2/25	G:3/25	NXA8
G:2/27	G:3/27	XWE
H:1/22	H:2/22	YOE
H:1/27	H:2/27	YWE
H:2/2	H:3/2	NYA12
H:2/3	H:3/3	NYA7
H:2/4	H:3/4	NYA6
H:2/5	H:3/5	NYA5
H:2/6	H:3/6	NYA4
H:2/7	H:3/7	NYA3
H:2/8	H:3/8	NYA2
H:2/9	H:3/9	NYA1
H:2/10	H:3/10	NYA0

H:2/11	H:3/11	MYDQ0
H:2/12	H:3/12	MYDQ1
H:2/13	H:3/13	MYDQ2
H:2/15	H:3/15	MYDQ3
H:2/16	H:3/16	MYDQ4
H:2/17	H:3/17	MYDQ5
H:2/18	H:3/18	MYDQ6
H:2/19	H:3/19	MYDQ7
H:2/21	H:3/21	MYA10
H:2/23	H:3/23	MYA11
H:2/24	H:3/24	MYA9
H:2/25	H:3/25	MYA8
H:4/2	H:5/2	A12
H:4/3	H:5/3	A7
H:4/4	H:5/4	A6
H:4/5	H:5/5	A5
H:4/6	H:5/6	A4
H:4/7	H:5/7	A3
H:4/8	H:5/8	A2
H:4/9	H:5/9	A1
H:4/10	H:5/10	A0
H:4/11	H:5/11	SDQ0
H:4/12	H:5/12	SDQ1
H:4/13	H:5/13	SDQ2
H:4/15	H:5/15	SDQ3
H:4/16	H:5/16	SDQ4
H:4/17	H:5/17	SDQ5
H:4/18	H:5/18	SDQ6
H:4/19	H:5/19	SDQ7
H:4/21	H:5/21	A10
H:4/22	H:5/22	RD-SHARE
H:4/23	H:5/23	A11
H:4/24	H:5/24	A9
H:4/25	H:5/25	A8
H:4/27	H:5/27	WR-SHARE
H:6/2	H:7/2	A12
H:6/3	H:7/3	A7
H:6/4	H:7/4	A6
H:6/5	H:7/5	A5
H:6/6	H:7/6	A4
H:6/7	H:7/7	A3
H:6/8	H:7/8	A2
H:6/9	H:7/9	A1
H:6/10	H:7/10	A0

H:6/11	H:7/11	SDQ0
H:6/12	H:7/12	SDQ1
H:6/13	H:7/13	SDQ2
H:6/14	H:7/15	SDQ3
H:6/16	H:7/16	SDQ4
H:6/17	H:7/17	SDQ5
H:6/18	H:7/18	SDQ6
H:6/19	H:7/19	SDQ7
H:6/21	H:7/21	A10
H:6/22	H:7/22	RD-SHAPE
H:6/23	H:7/23	A11
H:6/24	H:7/24	A9
H:6/25	H:7/25	A8
H:6/27	H:7/27	WR-SHAPE

A:1/7	F:23/10	XDQ2
A:1/8	F:23/13	XDQ3
A:1/9	E:23/10	XDQ6
A:1/10	E:23/13	XDQ7
A:1/13	C:14/10	YDQ2
A:1/14	C:14/13	YDQ3
A:1/15	B:13/10	YDQ6
A:1/16	B:13/13	YDQ7
A:1/29	B:21/13	XA8
A:1/30	B:23/13	XA12
A:1/31	B:21/10	XA9
A:1/32	B:23/10	XA13
A:1/33	B:21/6	XA10
A:1/34	B:23/6	XA14
A:1/35	B:21/3	XA11
A:1/39	B:21/14	YA..
A:1/40	B:23/14	YA12
A:1/41	B:21/11	YA9
A:1/42	B:23/11	YA13
A:1/43	B:21/5	YA10
A:1/44	B:23/5	YA14
A:1/45	B:21/2	YA11
A:1/69	F:23/3	XDQ0
A:1/69	F:23/6	XDQ1
A:1/70	E:23/3	XDQ4
A:1/71	E:23/6	XDQ5
A:1/74	C:14/3	YDQ0
A:1/75	C:14/6	YDQ1
A:1/76	B:13/3	YDQ4
A:1/77	B:13/6	YDQ5
A:1/90	B:16/13	XA0
A:1/91	B:18/13	XA4
A:1/92	B:16/10	XA1
A:1/93	B:18/10	XA5
A:1/94	B:16/6	XA2
A:1/95	B:18/6	XA6
A:1/96	B:16/3	XA3
A:1/97	B:18/3	XA7
A:1/100	B:16/14	YA0
A:1/101	B:18/14	YA4
A:1/102	B:16/11	YA1
A:1/103	B:18/11	YA5
A:1/104	B:16/8	YA2
A:1/105	B:18/8	YA6
A:1/106	B:16/2	YA3
A:1/107	B:18/2	YA7

A:1/111	F:21/10	XRD
A:1/113	F:21/6	YRD
A:1/117	F:21/4	XWR
A:1/119	F:21/2	YWR
B:11/4	B:13/2	SDQ4
B:11/7	B:13/5	SDQ5
B:11/11	B:13/9	SDQ6
B:11/14	B:13/12	SDQ7
B:13/1	F:11/8	CS-SYDATA
B:13/4	H:4/16	SDQ4
B:13/7	H:4/17	SDQ5
B:13/11	H:4/18	SDQ6
B:13/14	H:4/19	SDQ7
B:16/1	B:21/1	YSEL
B:16/4	H:4/7	A3
B:16/7	H:4/8	A2
B:16/9	H:4/9	A1
B:16/12	H:4/10	A0
B:16/15	F:17/3	STROBE
B:18/1	E:19/13	YSEL
B:18/4	H:4/3	A7
B:18/7	H:4/4	A6
B:18/9	H:4/5	A5
B:18/12	H:4/6	A4
B:18/15	B:21/15	STROBE
B:21/4	H:4/23	A11
B:21/7	H:4/21	A10
B:21/9	H:4/24	A9
B:21/12	H:4/25	A8
B:23/2	D:21/11	YA15
B:23/3	D:21/1	XA15
B:23/12	H:4/2	A12
C:12/1	F:22/8	CS-SXDATA
C:12/4	C:14/2	SDQ0

C:12/7	C:14/5	SDQ1
C:12/11	C:14/9	SDQ2
C:12/14	C:14/12	SDQ3
C:12/15	D:16/11	XSDIEN
C:14/4	H:4/11	SDQ0
C:14/7	H:4/12	SDQ1
C:14/11	H:4/13	SDQ2
C:14/14	H:4/15	SDQ3
C:14/15	D:16/	YSDIEN
D:13/2	D:13/4	MYDQ4
D:13/5	D:13/7	MYDQ5
D:13/9	D:13/11	MYDQ6
D:13/12	D:13/14	MYDQ7
D:16/3	E:15/2	XARBIT
D:16/6	E:15/5	YARBIT
D:16/10	E:11/9	YWRSEL
D:16/12	E:11/3	XWRSEL
E:11/1	E:12/16	XSEL
E:11/6	E:17/16	XRDSEL
E:11/10	E:11/12	YSEL
E:11/11	E:17/	YRDSEL
E:12/2	E:15/1	YSEL
E:12/5	E:12/16	YSEL
E:13/1	E:17/6	CS-YDATA
E:13/2	E:13/4	MYDQ0
E:13/5	E:13/7	MYDQ1
E:13/9	E:13/11	MYDQ2
E:13/12	E:13/14	MYDQ3
E:13/15	E:11/12	YDIEN
E:15/3	E:17/1	XSEL
E:15/4	E:12/2	XSEL
E:15/6	E:17/2	YSEL
E:15/4	E:12/5	XSEL
E:17/2	E:22/6	CE-XY

E:17/3	E:23/1	CS-XDATA
E:17/5	E:19/12	MYSEL
E:19/6	F:22/1[illegible]	MYSEL
E:23/2	E:23/4	NXDQ4
E:23/5	E:23/7	NXDQ5
E:23/9	E:23/11	NXDQ6
E:23/12	E:23/14	NXDQ7
F:12/1	D:23/14	CE-XY2000
F:12/4	D:23/13	CE-XY4000
F:12/9	D:23/12	CE-XY6000
F:13/1	F:13/[illegible]	XYARBIT
F:17/6	H:4/27	WR-SHARE
F:17/1	H:4/22	PD-SHARE
F:21/3	H:1/27	YWE
F:21/5	F:22/13	XWE
F:21/7	H:1/22	YOE
F:21/9	G:1/22	XOE
F:22/12	F:23/13	XDIEN
F:23/2	F:23/4	NXDQ0
F:23/5	F:23/7	NXDQ1
F:23/9	F:23/11	NXDQ2
F:23/12	F:23/14	NXDQ3
G:1/2	G:2/2	NXA12
G:1/3	G:2/3	NXA7
G:1/4	G:2/4	NXA6
G:1/5	G:2/5	NXA5
G:1/6	G:2/6	NXA4
G:1/7	G:2/7	NXA3
G:1/8	G:2/9	NXA2

G:1/9	G:2/9	NXA1
G:1/10	G:2/10	NXA0
G:1/11	G:2/11	NXDQ0
G:1/12	G:2/12	NXDQ1
G:1/13	G:2/13	NXDQ2
G:1/15	G:2/15	NXDQ3
G:1/16	G:2/16	NXDQ4
G:1/17	G:2/17	NXDQ5
G:1/18	G:2/18	NXDQ6
G:1/19	G:2/19	NXDQ7
G:1/21	G:2/21	NXA10
G:1/23	G:2/23	NXA11
G:1/24	G:2/24	NXA9
G:1/25	G:2/25	NXA8
G:1/27	G:2/27	XWE
G:2/22	G:3/22	XOE
H:1/2	H:2/2	NYA12
H:1/3	H:2/3	NYA7
H:1/4	H:2/4	NYA6
H:1/5	H:2/5	NYA5
H:1/6	H:2/6	NYA4
H:1/7	H:2/7	NYA3
H:1/8	H:2/8	NYA2
H:1/9	H:2/9	NYA1
H:1/10	H:2/10	NYA0
H:1/11	H:2/11	NYDQ0
H:1/12	H:2/12	NYDQ1
H:1/13	H:2/13	NYDQ2
H:1/15	H:2/15	NYDQ3
H:1/16	H:2/16	NYDQ4
H:1/17	H:2/17	NYDQ5
H:1/18	H:2/18	NYDQ6
H:1/19	H:2/19	NYDQ7
H:1/21	H:2/21	NYA10
H:1/23	H:2/23	NYA11
H:1/24	H:2/24	NYA9
H:1/25	H:2/25	NYA8
H:2/22	H:3/22	YOE
H:2/27	H:3/27	YWE
H:1/2	H:3/2	A12

H:5/3	H:6/3	A7
H:5/4	H:6/4	A6
H:5/5	H:6/5	A5
H:5/6	H:6/6	A4
H:5/7	H:6/7	A3
H:5/8	H:6/8	A2
H:5/9	H:6/9	A1
H:5/10	H:6/10	A0
H:5/11	H:6/11	SDQ0
H:5/12	H:6/12	SDQ1
H:5/13	H:6/13	SDQ2
H:5/15	H:6/15	SDQ3
H:5/16	H:6/16	SDQ4
H:5/17	H:6/17	SDQ5
H:5/18	H:6/18	SDQ6
H:5/19	H:6/19	SDQ7
H:5/21	H:6/21	A10
H:5/22	H:6/22	RD-SHARE
H:5/23	H:6/23	A11
H:5/24	H:6/24	A9
H:5/25	H:6/25	A8
H:5/27	H:6/27	WR-SHARE

D:23/12	F:12/9	CE-XY6000
D:23/13	F:12/4	CE-XY4000
D:23/14	F:12/1	CE-XY2000

Vita

Gennaro Cuomo was born on 28 August 1947 in New York City, New York. He graduated from Plainview High School, New York in 1965 after which he attended Nassau Community College, Garden City, New York. In May 1967, he entered the U.S. Air Force. In July 1968, he entered the United States Air Force Academy Preparatory School and was graduated from the USAF Academy in June 1973 with a Bachelor of Science degree in Electrical Engineering. Following graduation, he attended Undergraduate Navigator Training (UNT) at Mather AFB, California. Upon graduation from UNT, he entered Electronic Warfare Training (EWT) also at Mather AFB. After EWT, he was trained as an Electronic Warfare Officer (EWO) aboard a B-52H at Castle AFB, California. He was then assigned to Kincheloe AFB, Michigan from March 1975 through June 1977. Upon the closure of Kincheloe AFB, he was assigned to Ellsworth AFB, South Dakota as an Instructor EWO, from July 1977 through November 1980. He entered the Air Force Institute of Technology in December 1980.

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19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Local Area Network
Local Computer Network
Message Processors
Network Interface Device

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The object of this investigation was to design and construct two memory boards for the Digital Engineering Laboratory Network's (DELNET's) Universal Network Interface Devices (UNIDs). The UNID is a flexible message processor designed for computer communications network applications. The new memory boards incorporated the prototype microcomputer based message processor boards of the previous theses. Using the existing memory boards, new memory boards were designed, constructed, tested, and documented. The results of this effort were the elimination of unreliable RAM, the reduction in the number of circuit boards used in the UNID, and two operational UNIDs.

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